Data Decoder Assembly Implementation Status

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Twelve data decoder assemblies have been acceptance-tested, delivered to the Deep Space Network stations, and are undergoing installation/testing, and incorporation of field modifications in preparation for the Pioneer F mission. Eight additional data decoder assemblies are in different stages of testing and implementation. This article describes their present status.

I. Introduction

The original procurement for 12 data decoder assemblies (DDAs) to implement the prime *Pioneer F* stations has been completed with acceptance testing and shipment of the equipment to the designated stations (DSSs 11, 42, 51, 61, 71 and CTA 21). The units have been installed at the stations and are in various stages of test verification and operational testing.

An add-on procurement for eight additional DDAs for DSSs 12, 14, 42, 62 and one each for DSS 71 and CTA 21 is ahead of the originally planned schedule. Four units have passed acceptance testing, been shipped, and received at the designated station. Current scheduling shows that manufacturing and testing of the remaining four DDA units and spares should be completed early in 1972.

The multiple-mission telemetry (MMT) 1971-1972 configuration signal flow diagrams depicting the implementation of the DDAs at all DSSs are shown in Figs. 1 through 5.

II. Manufacturing/Acceptance Testing

The last four DDAs are in various stages of manufacturing and testing at the contractor's facility with one unit ready for acceptance testing. All units will be through acceptance testing by the middle of January with spares and special test equipment completed by the middle of February.

Final documentation is currently undergoing review by JPL and will be available by the end of March 1972.

III. Installation and Testing

All prime *Pioneer F* stations: DSSs 11, 42, 51, 61, and 71 have received and installed their DDAs. The units are currently undergoing extensive subsystem tests with the DDA test programs (Table 1). Preliminary *Pioneer F* operation programs have also been distributed to the prime stations to allow hardware/software compatibility testing in preparation for the February 1971 *Pioneer F* launch. Two DDAs were received at DSS 41 on December 10, and two at DSS 12 on December 7, 1971. Installation is currently underway on this equipment.

IV. Field Modifications

Since Motorola began shipping units to the overseas stations around the beginning of August, there have been six field modifications (FMs) sent to all stations to expand design capabilities and or to correct various design deficiencies. Modifications 1–5 have been implemented to the extent that the wiring changes have been incorporated and some borrowing (within the station) of integrated circuits (ICs) and component platforms has been necessary until modification kit parts are shipped to the stations. A summation of the field modifications is as follows by FM number:

(1) FM 1 to change number of bits from the SSA (increase from 3 to 5) used to provide information for proper operation of sequential decoding function during low signal-to-noise ratio (SNR). This affected the SSA coupler.

(2) FM 2 to replace missing wire for signal return of coax shield for SSA clock. This affected the interface panel assembly (backplane).

(3) FM 3 provides, to not set PIN OVERRATE FLAG when initializing DDA and to not generate INITIALIZATION or MEMORY RECALL INTERRUPTS when TCP is using indirect addressing. This affected the TCP/DDA coupler.

(4) FM 4 to change EOM address from 'EOM 33776' X'7FE' to 'EOM 37657' X'FAF'. This affected the TCP/DDA coupler.

(5) FM 5 to control plenum air flow through DDA (especially the temperature of the ID 4 computer).

(6) FM 6 to provide BIT ERROR count change to allow BIT comparison of p_k with P_K and either q_k with Q_K or q_k with $\overline{Q}_K$.

In addition to the current list of field modifications, it was determined several months ago that the then expansion read-only memory (ROM) design was not adequate for all sequential decoding cases. The original software simulation technique used to design the expansion ROM was not capable of eliminating low probability bugs, and so the problem was not discovered until the sequential decoding function was being proven with the first available hardware. The expansion ROM design has since been corrected and new hardware will be procured. The existing ROMs are capable of supporting the early *Pioneer F* mission phase with the replacement ROMs planned for installation in May 1972.

V. Failures

There have been several failures of Interdata Model 4 mother boards and daughter boards. These have been repaired on site in the cases when the station personnel had test equipment and replacement parts available. In almost every case the failure was an IC and attributable to infant mortality because the ICs used in the Interdata Model 4 are of unscreened commercial quality.

There have been no reported failures from the field of screened ICs or discreet components used in the Interface Panel Assembly.

Table 1. DDA test programs

Title	Also known as	Description
Resident telemetry and command processor assembly (TCP) software (DDA test)	—	—
Model 4 test program	—	This program exercises the DDA central processing unit (CPU) and sends diagnostics to the TCP via the TCP coupler.
Memory parity	Memory test, memcheck, Memory parity test	This program writes and reads core and checks for discrepancies. Diagnostics are sent to the TCP.
Special instructions (common) & DDB	Decode data buffer (DDB) - Common special instructions and DDB - DDB test program	Exercises the DDB and sends errata to the TCP. This tests common special firmware (see DOI-5093-TP).
Frequency and Timing Subsystem (FTS) and Symbol Synchronizer Assembly (SSA) coupler	—	Exercises FTS and SSA couplers and sends diagnostics to the TCP.
TCP emulator & related special instructions	TCP emulator	Checks both software and firmware sequences for EOM, PIN, POT, and SKS. Errata transferred to the TCP.
Data decoding and handling	Functional test	This program acquires sync and decodes the symbol frames and implements transfer of decoded and erasure data to the TCP.
Sequential decoder statistics	SEQSTAT	Decodes 10K frames and provides coder statistics for generation of performance curves.
Self check	Self test	Detailed interface check.

EOM = energize output M; PIN = parallel input; POT = parallel output; SKS = skip if not set.

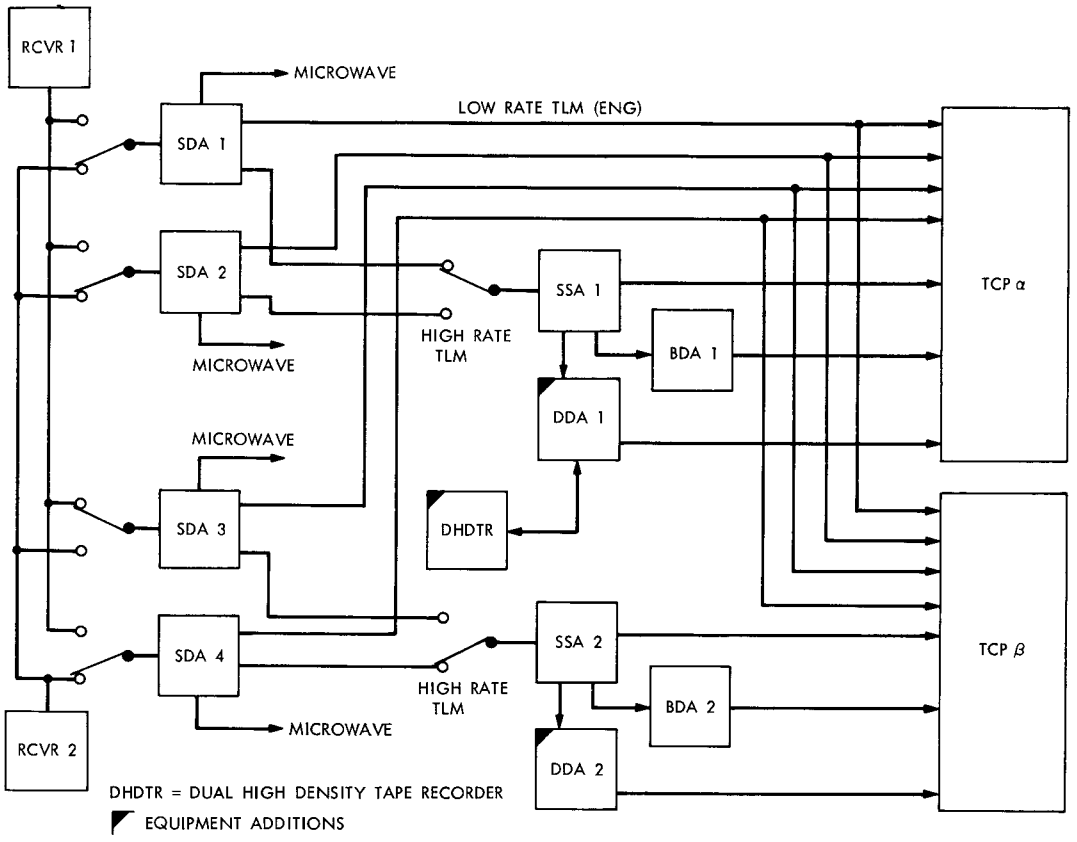

Fig. 1. MMT 1971-1972 configuration signal flow diagram (CTA 21)

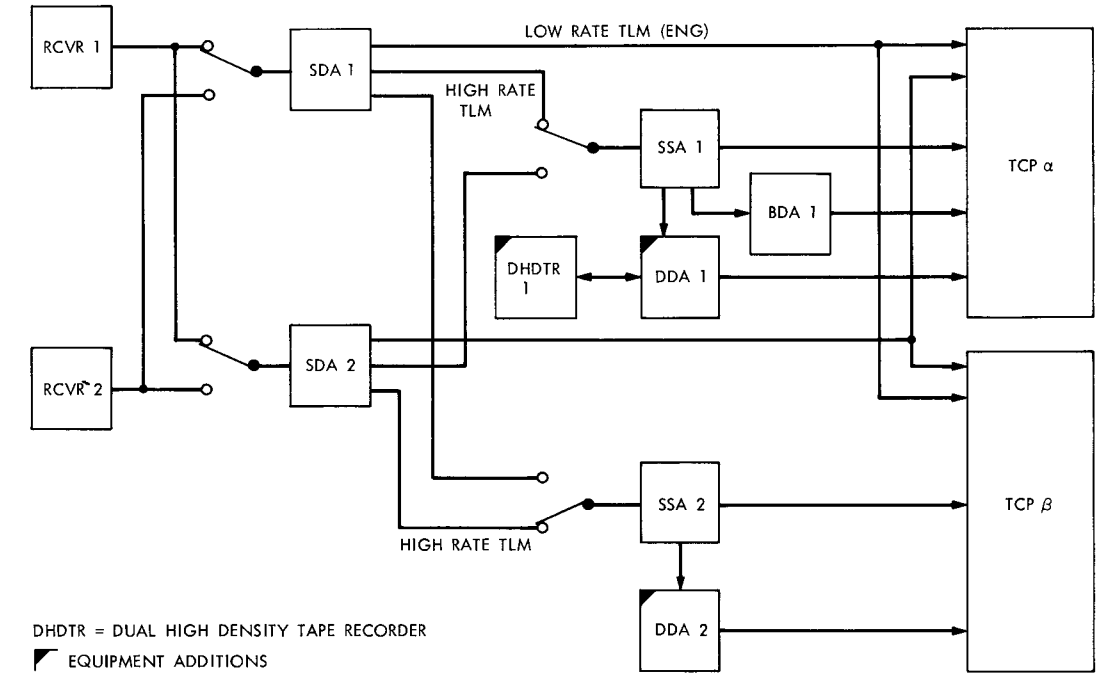

Fig. 2. MMT 1971-1972 configuration signal flow diagram (DSS 71)

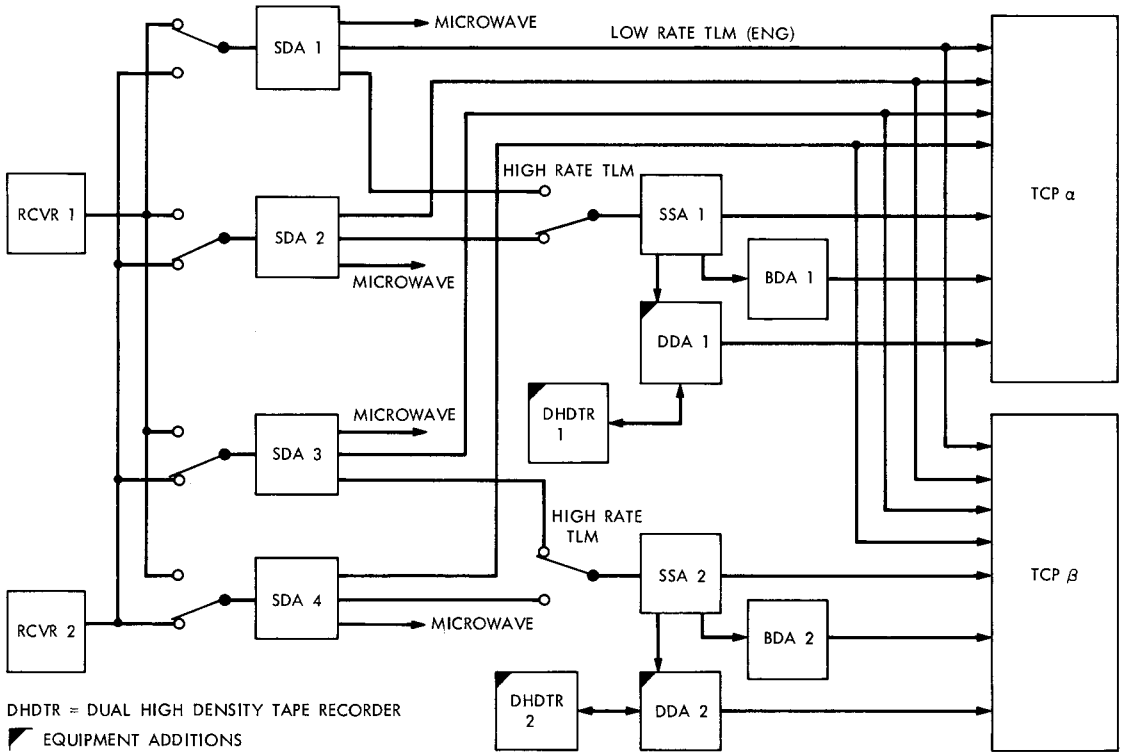

Fig. 3. MMT 1971-1972 configuration signal flow diagram (DSS 14)

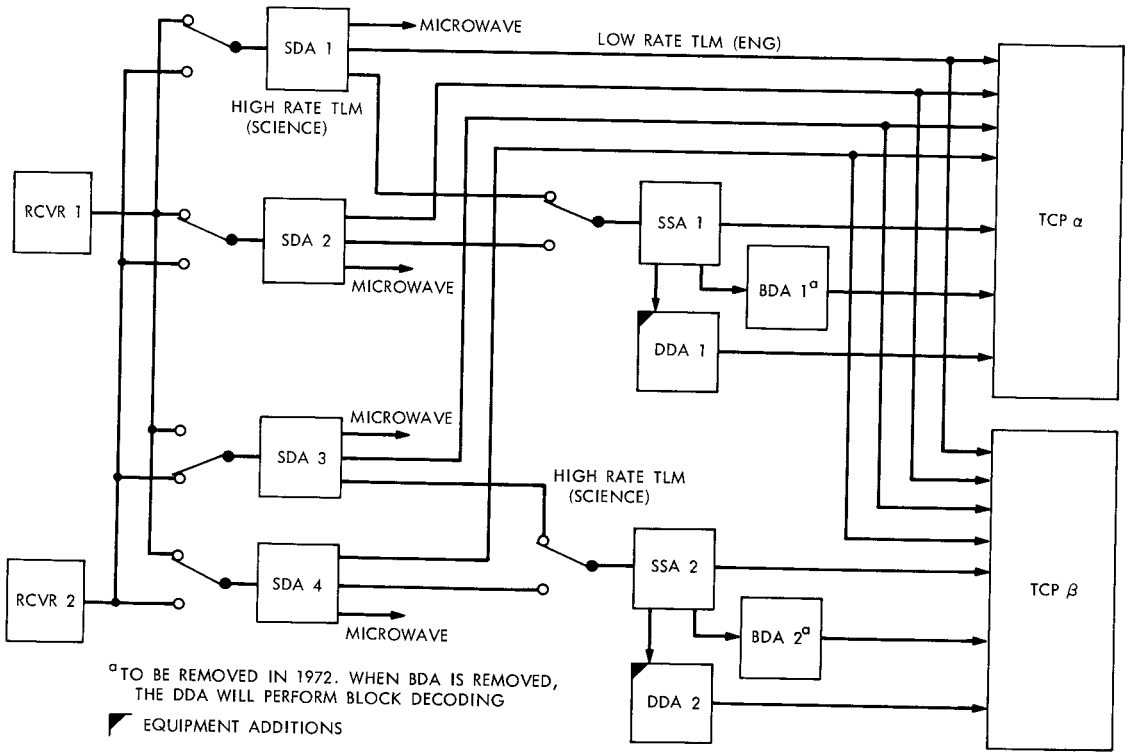

Fig. 4. MMT 1971-1972 configuration signal flow diagram (DSSs 12, 41, and 62)

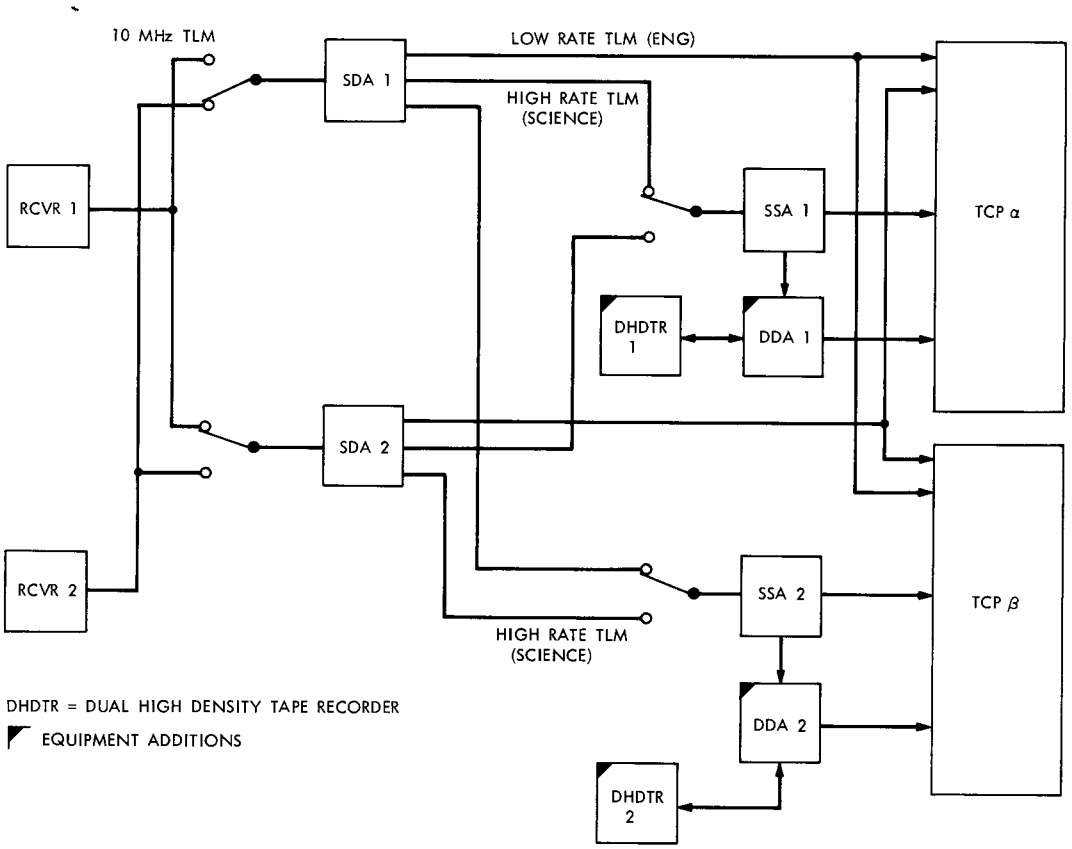

Fig. 5. MMT 1971-1972 configuration signal flow diagram (DSSs 42 and 61)