DSN Programmed Oscillator Development

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This article describes the development of a programmed oscillator utilizing a Dana Laboratory Digiphase synthesizer Model 7010-S-179. A brief description of the synthesizer characteristics and the technique for digital control is given. With this synthesizer, the programmed oscillator has the capability to be controlled at rates and ranges required for tracking outer-planet probes and yet provide the resolution and stability required for narrow-loop bandwidth receivers.

I. Introduction

The development of a new technique to program frequency using a Dana Laboratory Model 7020-103 Digiphase synthesizer was described in Ref. 1. The engineering model that was built demonstrated the feasibility of using this technique. However, to provide the capability required for the DSN, an improved synthesizer, Model 7010-S-179, was developed by Dana Laboratory. This article describes the increased capability of the new synthesizer and the assembly developed to control it.

II. Synthesizer

The increased capability of the Model 7010-S-179 synthesizer (Fig. 1) is shown in Table 1. Each of these items is discussed in more detail below.

A. Frequency Resolution

Model 7020-103 (Ref. 2) by itself provides frequency resolution of 1 Hz. However, fractional-hertz resolution was obtained with this synthesizer in the remote control mode. This capability was described in Ref. 1. The Model 7010-S-179 (Ref. 3) incorporates fractional-hertz resolution with local control to 10^{-6} decade. The inclusion of fractional-hertz resolution in the synthesizer eliminates the need to use the rate multiplier technique described in Ref. 1 to externally generate fractional-hertz control.

B. Phase Increments

In Model 7020-103, the numbers in each decade, down to the 10-Hz decade, are sampled by the loop each 10 μsec. An increase of one digit in the 10-Hz decade during one of these sample periods would then be an incremental change in phase of $(2\pi)(1)(10)(10^{-5})$ or $2\pi \times 10^{-4}$ rad. This represents about an 8-deg incremental change in phase at X-band in the Block 4 receiver–exciter. The Model 7010-S-179 synthesizer has been modified to sample down to the 1-Hz decade (Fig. 2). This modification then reduces the incremental phase change at X-band to less than 1 deg.

C. Long-Term Phase Stability

Two modifications to the synthesizer have been developed to improve the long-term phase stability. First, the temperature stability of the components in the digital

loop have been improved; second, the input reference frequency has been changed from 5 to 50 MHz. Utilizing 50-MHz permits the use of a simpler and more stable mechanization for the generation of the 100-kHz clock. Both these changes have improved the stability by an order of magnitude.

D. Input Reference Standard

The 50-MHz reference standard now being used is the most stable reference available from the hydrogen maser. The use of this reference improves the total system stability directly and the synthesizer stability indirectly as mentioned in Sect. C. above.

E. Output Frequency Monitor

Monitoring outputs that indicate whether or not the synthesizer is responding correctly to the programmed input have been provided in Model 7010-S-179. This is described in more detail later.

III. Control Assembly

First, the Model 7010-S-179 synthesizer will be examined. The output frequency is determined by the input BCD number into each of the decades from 10^7 to 10^{-6}. This number can be selected from the front panel switches in the local control mode or from an external device in the remote control mode (Fig. 2). This input number is sampled once each 10 μsec, the sampling interval being controlled by the 100-kHz clock. The sampling occurs during one-half of each clock cycle, while the other half of each cycle is reserved for number changes (Ref. 1). This is illustrated in the timing diagram (see Fig. 6), which shows the number changes occurring during the half cycle when the 100-kHz clock is low. Since number changes must be synchronized with the clock, the synthesizer can only be used in the remote control mode when the frequency is programmed.

Next, consider the digital loop within the synthesizer. The reference numbers for the loop control are obtained from the 10^0 to 10^7 decades. Since these numbers are sampled 10^5 times per second, when the number in the 10^0 decade is increased by one during one of these sampling periods, it represents an incremental change in the output of the synthesizer of $2\pi \times 10^{-5}$ rad (<1 deg at X-band). When the number in the 10^0 decade is incremented during one of the sampling periods and retained at this higher number, then the incremental change is still $2\pi \times 10^{-5}$ rad, but the frequency has been increased by 1 Hz. Incrementing the reference number once each second and retaining this increased value would then provide a frequency change at a rate of 1 Hz/sec. Pursuing this one step further, when the number in the 10^0 decade is increased by one each sampling period and retained, the incremental changes are still only $2\pi \times 10^{-5}$ rad each, but the frequency changes at a rate of 10^5 Hz/sec. Using this technique, frequency changes at a rate of 10^5 Hz/sec at the synthesizer output can be obtained with incremental changes of less than 1 deg at X-band. Since incrementing the frequency at each sample period results in a frequency rate of 10^5 Hz/sec, lower rates can be generated by increasing the frequency less often than each sample period.

To compute frequency numbers for each 10-μsec interval and insert these numbers into the synthesizer is beyond the capability of a computer. The control assembly, therefore, has been developed to provide this capability. Since doppler frequency changes are relatively slow, the program can be divided into linear segments, each much greater than 10 μsec long. The computer can then calculate these linear frequency rates ($\dot{F}$), and the control unit provides the logic circuitry necessary to convert these frequency rates to synthesizer control input numbers for each 10-μsec sample interval.

To illustrate the methods of obtaining fractional-hertz control and of generating a linear frequency ramp, consider the following simplified mathematical model (Fig. 3): The input reference phase ($\Delta\phi_{\text{ref}}$) to the loop can be expressed as

$$\Delta\phi_{\text{synth}} = \Delta\phi_{\text{ref}} = \Delta\phi_0 + \sum_{i=1}^{n} \Delta\phi_i$$

where

$\Delta\phi_0$ = initial phase

$\Delta\phi_i$ = incremental change in phase

n = number of incremental changes

However, the initial phase and incremental phase changes are

$$\Delta\phi_0 = F_0 \Delta t_i$$

$$\Delta\phi_i = \Delta F_i \, \Delta t_i$$

where

F_0 = initial frequency

ΔF_i = incremental change in frequency

Δt_i = time period between increments (10 μsec)

Then

$$\Delta\phi_{\text{synth}} = \Delta\phi_{\text{ref}} = \sum_{i=1}^{n} F_0 \Delta t_i + \Delta F_i \, \Delta t_i$$

This is accomplished in the following manner: The initial frequency (F_0) and the frequency ramp ($\dot{F}$) numbers are inserted into the control unit. The frequency ramp, or incremental frequency changes, are accumulated and combined with the initial frequency at clock intervals. The combined frequency numbers are then inserted into the synthesizer at these same clock intervals. Within the synthesizer, the frequency numbers are then accumulated at the 100-kHz clock rate to provide the phase reference for the digital loop.

To illustrate the phase tracking response of the synthesizer to an incremental frequency step, consider a step change of 1 Hz applied to the simplified model of Fig. 3. (It is assumed the loop is initially in a steady-state condition prior to the frequency change.) This results in an additional reference phase increment $\Delta\phi_{\text{ref}}$ equal to $2\pi \times 10^{-5}$ rad. The loop output phase response $\Delta\phi\,(t)_{\text{synth}}$ for that of the model of Fig. 3 is as follows:

$$\Delta\phi\,(s)_{\text{synth}} = \left(\frac{K_T}{N}\right) \frac{1 + \tau s}{s^2 + \frac{K_T}{N}\tau s + \frac{K_T}{N}} \left(\frac{\Delta\phi_{\text{ref}}}{s}\right)$$

Loop parameters of the model are:

$K_T = K_A K_V K_D$ = open-loop gain

K_A = loop amplifier gain $\cong 500$

$\frac{K_D}{N}$ = phase detector gain $\cong 5.8$ V/rad

K_V = VCO gain $\cong 2\pi \times 10^6$ rad/sec/V

$N = 500$ for this example

τ = loop time constant (165 μsec)

δ = loop damping factor (assumed = 0.707)

The time response $\mathcal{L}^{-1}\,[\Delta\phi\,(s)_{\text{synth}}]$ is as follows:

$$\Delta\phi\,(t)_{\text{synth}} = \left[1 - \epsilon^{-\alpha t}\left(\cos\omega_D t + \frac{\alpha}{\omega_D}\sin\omega_D t\right)\right]\Delta\phi_{\text{ref}}$$

where

$$\alpha = \delta\sqrt{K_T/N}$$

$$\omega_D = \sqrt{\frac{K_T}{N} - \alpha^2}$$

For this example,

$$\alpha \cong 6060$$

$$\omega_D \cong 6060 \text{ rad/sec}$$

The time response $\Delta\phi\,(t)_{\text{synth}}$ is shown in Fig. 4. Note that the synthesizer VCO output phase settles to that resulting from the new programmed frequency $F_0 + 1$ Hz within approximately 1000 μsec.

Although a time lag occurs, the synthesizer VCO must track the input reference phase generated by integration of the frequency control number. If no further frequency increments are applied, the loop phase tracking error settles to less than that value defined by the sample rate, since the loop is corrected at that rate. Going one step further, if the frequency is incremented by 1 Hz every clock period, the synthesizer output lags the computed reference phase by approximately 0.001 rad. This corresponds to a sweep rate of 100,000 Hz/sec. When the frequency ramp is removed, the output phase of the synthesizer converges with that of the reference phase computed and settles to that value within approximately 1000 μsec.

The frequency ramp is generated in the control assembly, as derived from manually selected or computer-generated rate control numbers. The functional units which accomplish this task are described individually below.

A. Frequency Control Register

Frequency BCD format is sent to the synthesizer from the frequency control register each clock cycle (10 μsec) (Fig. 5). The frequency information stored in this register is the algebraic sum of two inputs: the initial frequency and the incremental/decremental change in frequency. The initial frequency BCD information for each decade from 10^{-6} to 10^{7} is sent to the register either from the manual control select switches of the control assembly or from the computer. The incremental change in frequency is derived from the rate accumulator and is furnished to one of the 10^{-5} to 10^{-1} decades, depending on the rate of frequency change. To provide the capability of incrementing or decrementing the frequency, the frequency control register consists of decade UP/DOWN counters. Polarity information is received by the register along with an output pulse from the rate accumulator. The polarity selected determines whether the pulse from the rate accumulator will increase or decrease the frequency number in the frequency control register.

B. Rate Accumulator

The rate accumulator integrates the selected five-significant-figure rate number and produces a pulse rate output equal to the rate number. The output pulses increment the frequency control register in fractional-Hz increments, as determined by the decade of operation (Table 2). Similar to the frequency control inputs, the rate control numbers can be derived from manual BCD selectors or the computer. The five significant figures used are based on the clock rate (100 kHz). This means that 1 to 99,999 pulses each second as selected are generated over the 100,000 10-μsec sample periods (1-sec interval). This method of generating the frequency ramp approximates a smooth function, since the incremental step changes never exceed $2\pi \times 10^{-5}$ rad and the pulses are approximately evenly spaced over the 1-sec period.

To accommodate all known tracking requirements, five ranges are available. The range selected is identified by the position of the decimal point in the range rate manual control select switch or corresponding display. Although the frequency control resolution (Table 2) is reduced by a factor of 10 operating in the next higher range, the synthesizer control loop incremental step changes are still maintained at the minimum size of $2\pi \times 10^{-5}$ rad.

Generating the pulse to update the frequency control register is accomplished by using a BCD adder and an accumulator register to sum and accumulate the selected BCD rate every 10 μsec (Fig. 6). This is accomplished in the following manner: The input frequency rate number ($\dot{F}$) is stored in the rate register. These numbers are sampled each 10 μsec in sequence, as shown in the timing diagram. The timing diagram shows the timing pulses used in sampling these numbers. Pulse T1 enables the least-significant BCD number to be added to its related previous value stored in the accumulator register. The result of the add operation is stored as the new value along with any carry which may have resulted. This value is then shifted, and the next higher significant digit is sampled. The process continues until all five rate numbers are sampled to complete a full add cycle. Note that a full add cycle occurs within 2.5 μsec. A carry resulting from the most-significant number addition is the output pulse desired. This pulse then increments or decrements the proper frequency control register decade as listed in Table 2.

C. Acquisition Sweep

For an application such as acquisition, it is desirable to have the capability of triangular sweep. This capability is included in the control unit and provides a frequency sweep between predetermined upper and lower limits. Fig. 7 is a simplified diagram showing the frequency control register compared with the upper or lower stored limit, as determined by the polarity. When the digital comparator logic senses equality, a signal is sent to the polarity control logic to momentarily clear and stop the rate accumulator, force a polarity reversal, and then enable the rate accumulator to continue. Limits are selectable over the operating range of the synthesizer with resolution of 10^{-4} Hz. The figure is shown with rate range 1 selected.

D. Monitoring

It is necessary to verify that the output frequency of the synthesizer agrees with the input program. The output frequency cannot be counted directly to the accuracy required; therefore, it is necessary to use indirect means of monitoring (Fig. 8). The alternative used is to verify that the programmed frequency numbers (monitor 1) are being entered into the synthesizer and that the synthesizer loop remains locked. The control assembly includes the capability to read and store the synthesizer phase computer BCD codes (loop control inputs) at the station 1-sec tick (monitor 2). These values can, in turn, be sent to the computer for comparison with the predicted values. The synthesizer loop phase detector output is also monitored. Failure of the synthesizer VCO to track the phase computer is signaled by a digital pulse indicating the loop phase error has exceeded normal operating limits (monitor 3).

E. Controls and Displays

As mentioned previously, the synthesizer can be controlled remotely in the manual mode, although the primary remote mode is computer-controlled. The manual capability is included for operator control as a backup mode and for local checkout and fault localization when it is not desirable or possible to use the computer. Controls for the manual mode of operation are located on the front panel of the control assembly (Fig. 9). Commands to display or enter selections are dialed up on a coded selector switch, and the display or load pushbutton is enabled. In the load (enter) mode, the operator depresses the enabled load pushbutton, which stores the related BCD digital codes from the front panel selector switches. In the read mode, the display pushbutton is enabled, resulting in the selected display of frequency or sweep limits and GMT time or rate, as indicated on the command selector switch. The synthesizer control frequency displayed is that value present at the last station 1-sec tick.

Sweep rates entered are transferred to control latches at the next station 1-sec tick. Sweep ON/OFF and polarity selected are also transferred to control latches on the next station 1-sec tick. Sweep controls consist of RUN (ON/OFF), SWP (ON/OFF), and POLARITY (+/−). SWP ON enables the triangular sweep in frequency by enabling a polarity reversal when the preselected upper frequency limit and lower frequency limits are reached. This provides selection of a sweep window for automatic acquisition. RUN ON enables the rate accumulator operation producing the sweep rate (Hz/sec) selected and loaded in the rate control register. In the RUN mode, i.e., SWP OFF, the limits are disabled, inhibiting automatic polarity reversal. This is the doppler tracking mode.

An additional manual control will be added to the programmed oscillator control to allow the operator to preset sweep commands to be initiated at a desired GMT time. The selected rate and polarity will be initiated when station GMT time matches the stored value at the station tick.

F. Computer Interface

Data transfer to and from the programmed oscillator (PO) is in 8-bit bytes. Command and PO ID codes are sent first for register addressing in the PO, with data bytes following. Fig. 10a is a simplified diagram of the interface.

Data transmitted to the PO are stored in latches, and the latches are sampled on the station 1-sec tick in order to produce frequency corrections synchronous with the station clock. In the "tracking mode" (SWP OFF), the commands to load the frequency control register control decades and the rate control register control decades and the commands to initiate RUN are decoded, and corresponding data are transferred to latches. The registers that control the synthesizer are then loaded from these latches at the next 1-sec tick. Commands to stop a sweep are instantaneous (within 1 μsec after command is received).

Data transmitted to the computer are stored in latches and transferred one byte at a time (8 bits). The computer program sends a "read" command, which specifies the data requested and the number of bytes associated with the data. These data will be valid for the time tag related to the last 1-sec station tick.

Received 8-bit bytes, containing two BCD control codes each, are received sequentially from the computer and steered to storage latches in the PO, based on the value of a byte counter. The following is a description of the byte counter used for steering the data (8-bit bytes) to the addressed storage latch in the PO control registers (Fig. 10b).

The byte control word is a 3-bit code that sets the byte counter to the specified initial starting state. The counter output BCD code is decoded to the equivalent decimal value, thus enabling one of the 7 lines used for steering the subsequently occurring data strobe to the appropriate storage latch. For each successive value of the counter during multiple byte transfers, 8 bits are stored. The byte counter value is forced down 1 count with each 8-bit byte transfer, as signaled by a response RSP followed by a data ready RDY cycle of the interface control signals.

The first 8-bit byte received from the computer interface is the byte control word. This byte control word is stored in the byte counter in accordance with the number of data bytes to follow. The RCV/XMT control logic generates the data strobe, which is, in turn, steered by the successive value of the byte counter as it decrements by 1 for each data byte transferred. This is shown in the timing diagram of Fig. 11.

Data transfer can be terminated with the byte counter forced to zero (0), as accomplished by removing the computer stimulus (STC). Thus, any one of the byte latches may be addressed individually as well as sequentially. In this instance, the byte counter is set to the value desired with a data transfer of one byte following. After the RSP signal is received, the STC signal is removed to terminate transfer.

A typical data transfer from the computer to the PO is as follows: The computer transmits a coded command with the PO unit ID code concurrent with a computer stimulus (STC). The command is one of the 15 commands to load or read PO registers. This command is sent in BCD code on the 8 bi-directional data lines (4 bits containing command and 4 bits containing unit ID). If the unit ID is correct, the PO responds with a response to the stimulus (STC) and stores the command. The decoded command results in an enabling signal to the set of latches that are to receive data. In the case of a read command, transmit gates are enabled.

As a result of the response signal sent to the computer interface, the computer loads the interface lines with the byte count associated with the number of 8-bit bytes to follow and sets the data RDY bit. The byte control word

is recognized as such by the PO by a byte control code sent on the function lines C8 and C9. The byte control code enables a strobe to load the byte counter. The RSP signal is removed upon detection of the RDY signal. Subsequent byte transfers are coded as data bytes on C8 and C9 and occur with each successive cycle of RSP → RDY → $\overline{\text{RSP}}$ → $\overline{\text{RDY}}$ until the byte counter has decremented to zero, as illustrated in the timing diagram (Fig. 11).

IV. Packaging

The control assembly hardware is mounted in a 19.5-in. cabinet chassis that occupies 5.5 in. of panel space (Fig. 9). The front panel contains controls that are used in the manual control mode, as well as numeric displays used in either the manual or the computer control mode. Two LED numeric displays are used, one containing 14 digits and the other containing 6 digits. The 14-digit display reads out on command, either manually or from the computer, the upper and lower frequency sweep limits and the frequency input to the synthesizer from the control unit at a 1-sec sample rate. The 6-digit displays read out on command GMT or frequency sweep rate.

Fig. 9 shows the control assembly with the top cover removed. The compartment with the louvered cover contains the power supplies. Two rows of digital subassemblies can be seen. Wire wrap plug-in subassemblies are used to divide the control logic into separate functional elements and still provide high-density packaging. The use of functional subassemblies simplifies maintenance by reducing field troubleshooting to subassembly substitution until the defective plug-in is determined. One of the digital control plug-in cards is shown in Fig. 12 with the integrated circuits and with a plastic cover to protect the wire wrap pins from damage during handling.

V. Concluding Remarks

A PO has been developed that has the capability to be controlled at rates and ranges required for tracking outer-planet probes and yet provide the resolution and stability required for narrow-loop bandwidth receivers. This PO is being used in the Block 4 receiver–exciter, as well as in the exciter for the time sync. At the present time, the time sync is operational, and the PO is performing as predicted.

References

1. Wick, M. R., "Programmed Oscillator Development," *The Deep Space Network,* Space Programs Summary 37-66, Vol. II, pp. 127–132, Nov. 30, 1970.
2. Gillette, G. C., "The Digiphase Synthesizer," *Freq. Technol.*, Vol. I, No. 8, Aug. 1969.
3. *Dana Model 7010-S-179 Digiphase Frequency Synthesizer,* Dana Laboratory Publication 980428-S-179, July 1971.

Table 1. Synthesizer capability

Characteristic	Model	
	7020-103	7010-S-179
Frequency resolution, Hz	1	10^{-6}
Phase increments, 2π rad	10^{-4}	10^{-5}
Long-term phase stability, deg phase/°C	10.0	0.1
Input reference standard	5	50
Output frequency monitor available	No	Yes

Table 2. Rate accumulator ranges

Range	Control register decade	Range rate, Hz/s
1	10^{-5}	0.00001– 0.99999
2	10^{-4}	0.0001 – 9.9999
3	10^{-3}	0.001 – 99.999
4	10^{-2}	0.01 – 999.99
5	10^{-1}	0.1 –9999.9

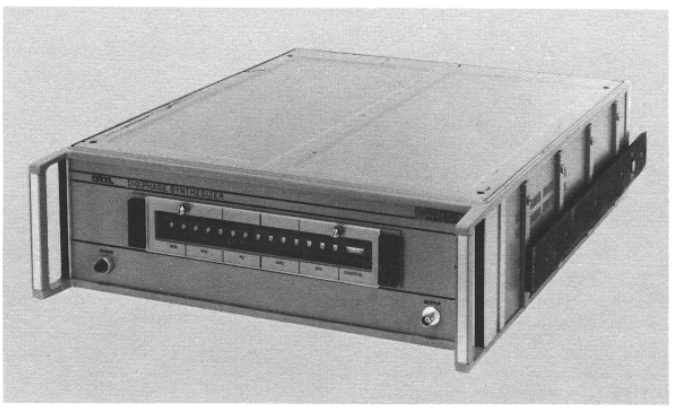

Fig. 1. Dana 7010-S-179 Digiphase frequency synthesizer

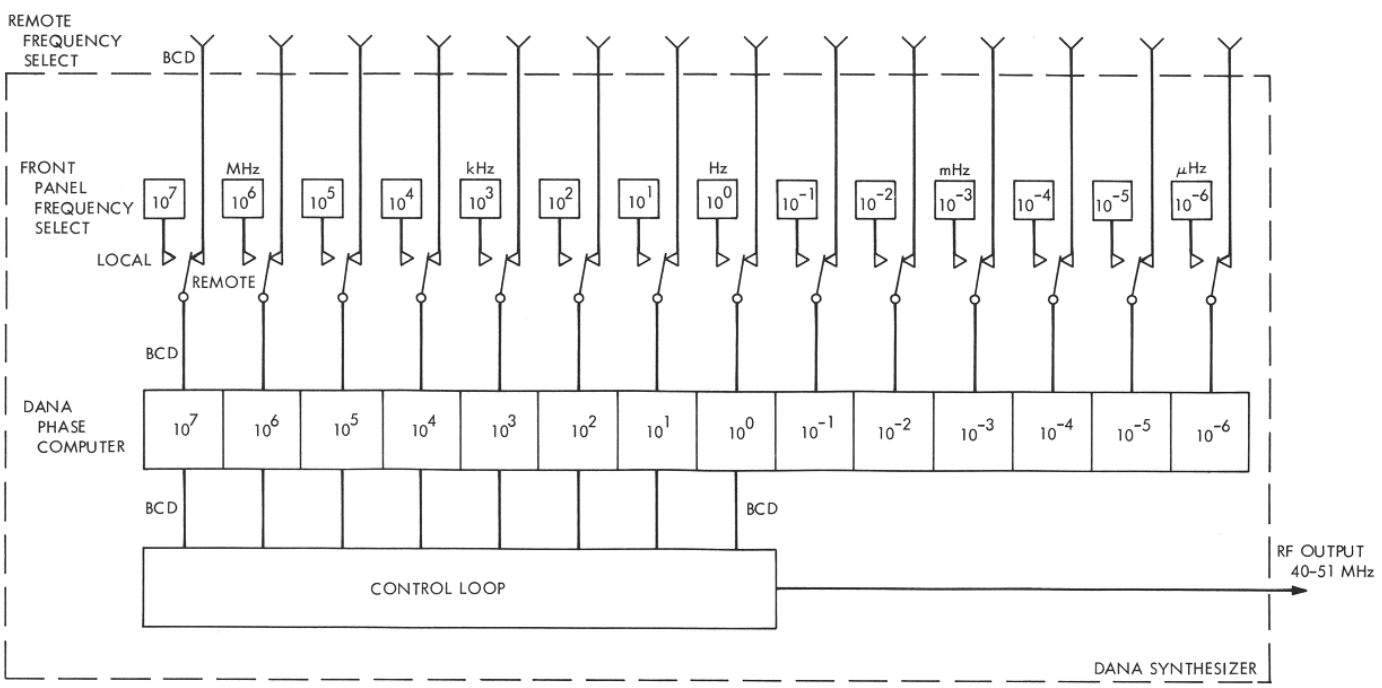

Fig. 2. Dana synthesizer control

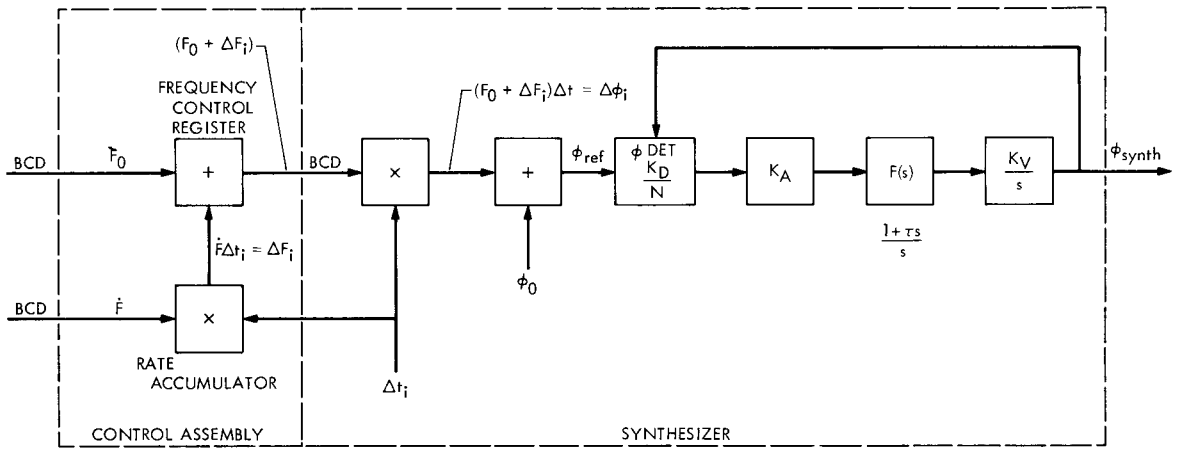

Fig. 3. Dana loop digital control

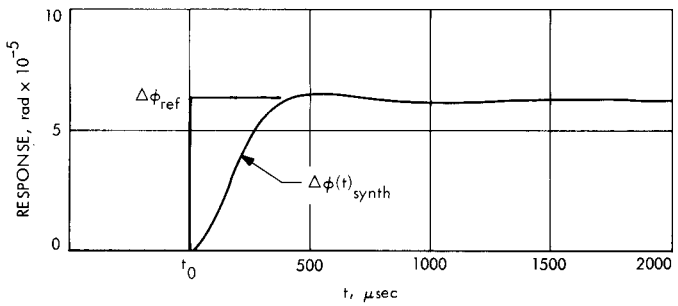

Fig. 4. Synthesizer model output response

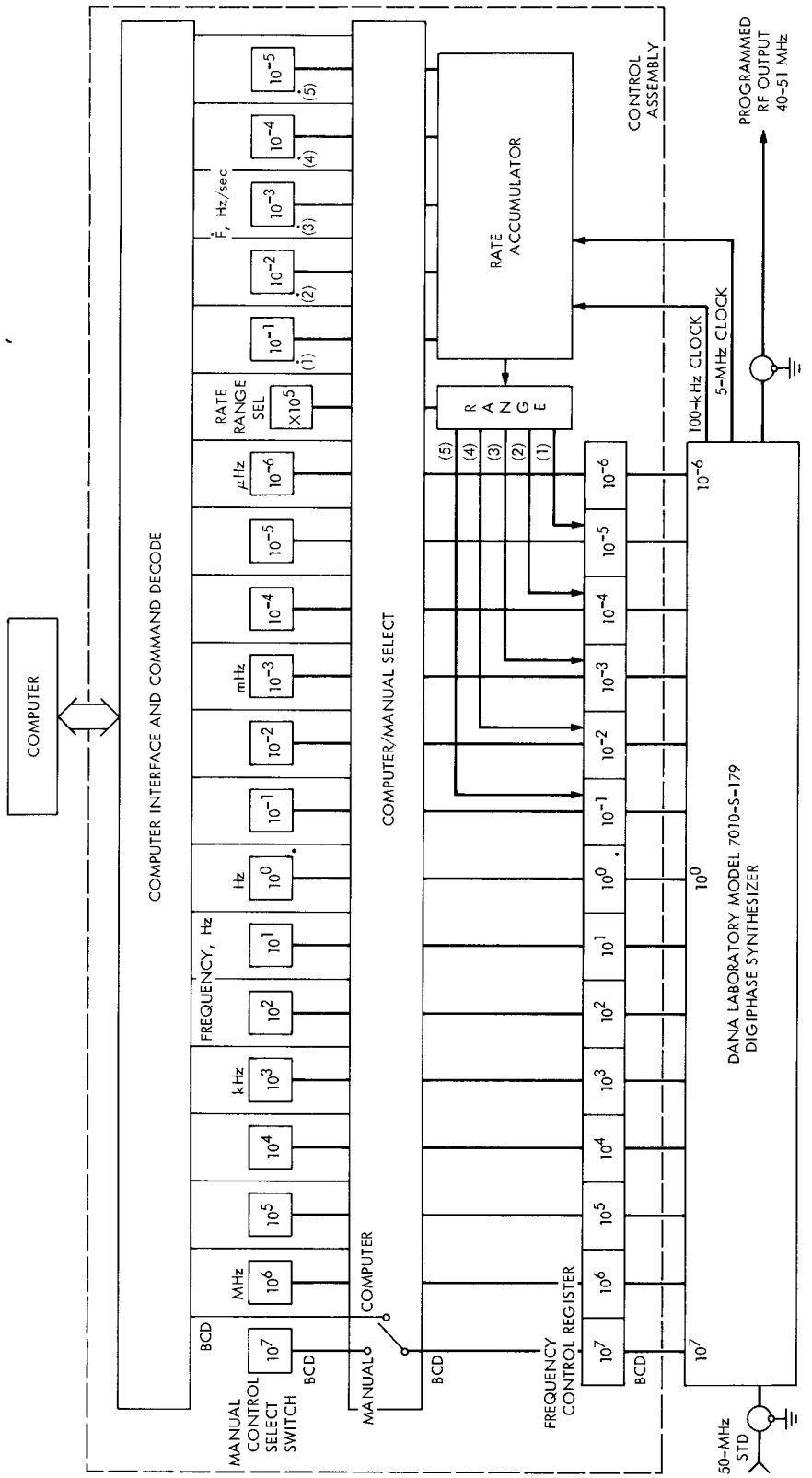

Fig. 5. Control assembly

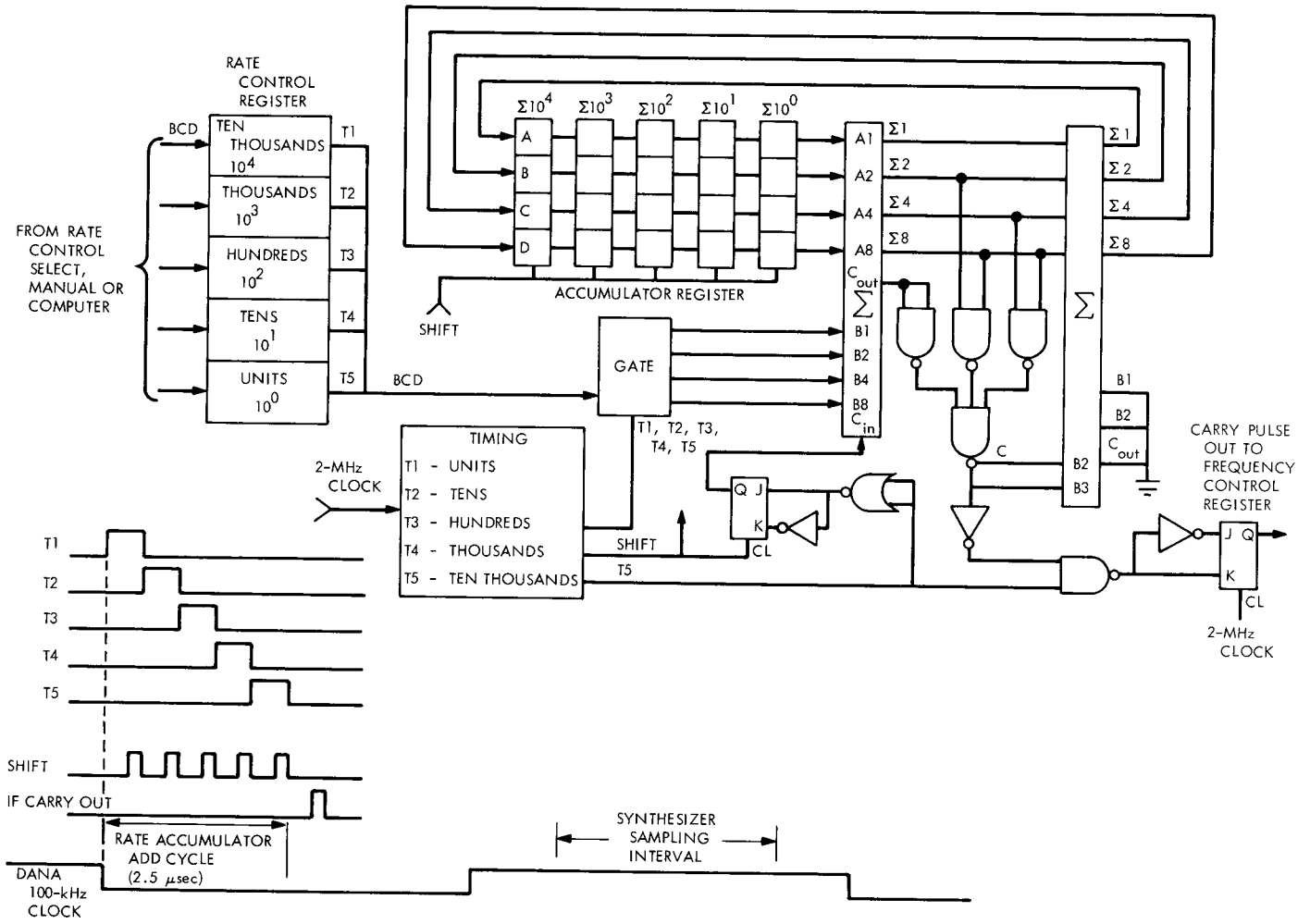

Fig. 6. Rate accumulator

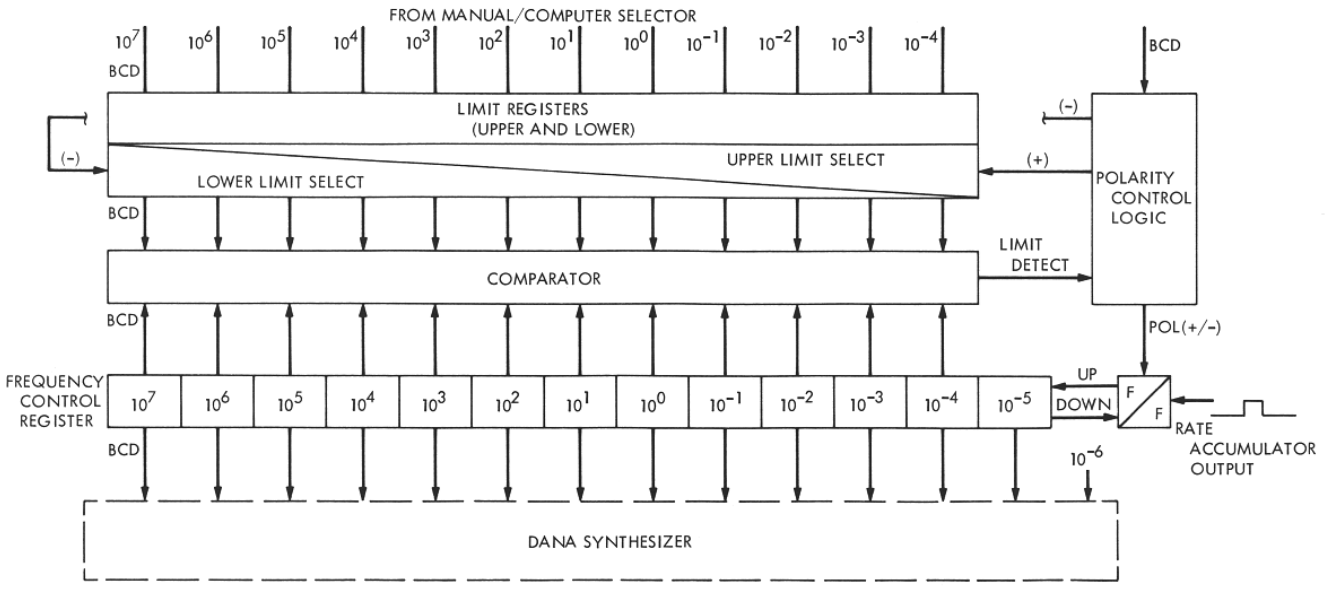

Fig. 7. Acquisition sweep control

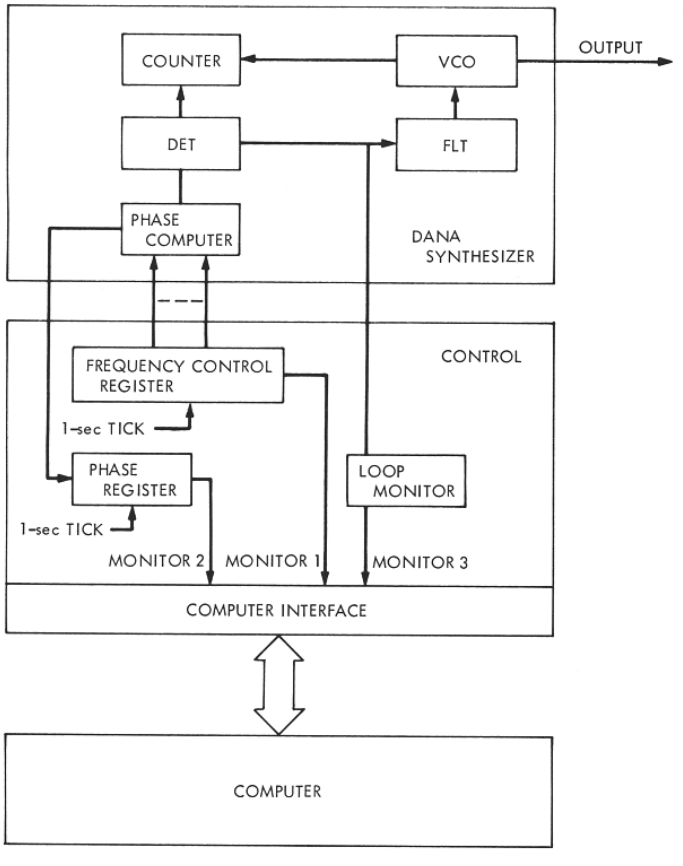

Fig. 8. Digital control assembly

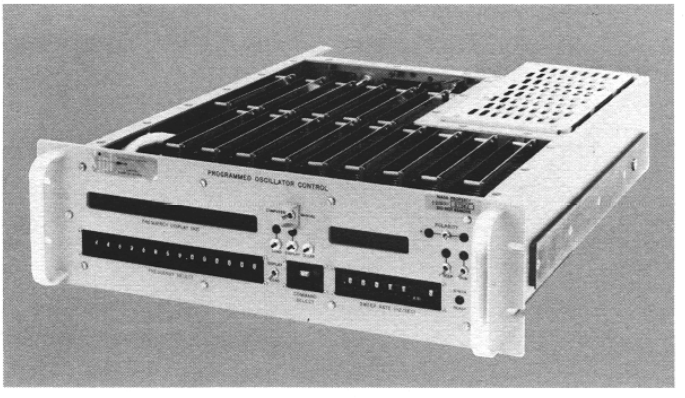

Fig. 9. Frequency monitor

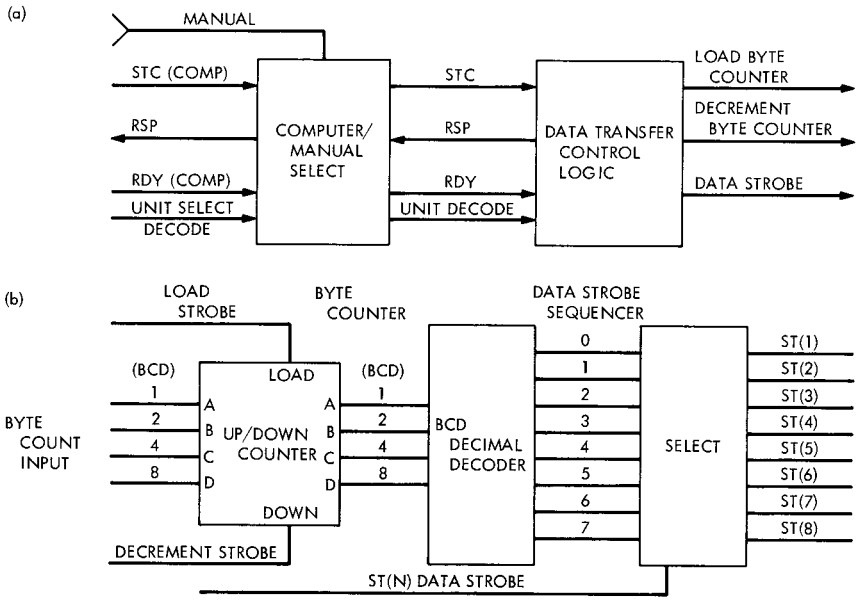

Fig. 10. Computer interface

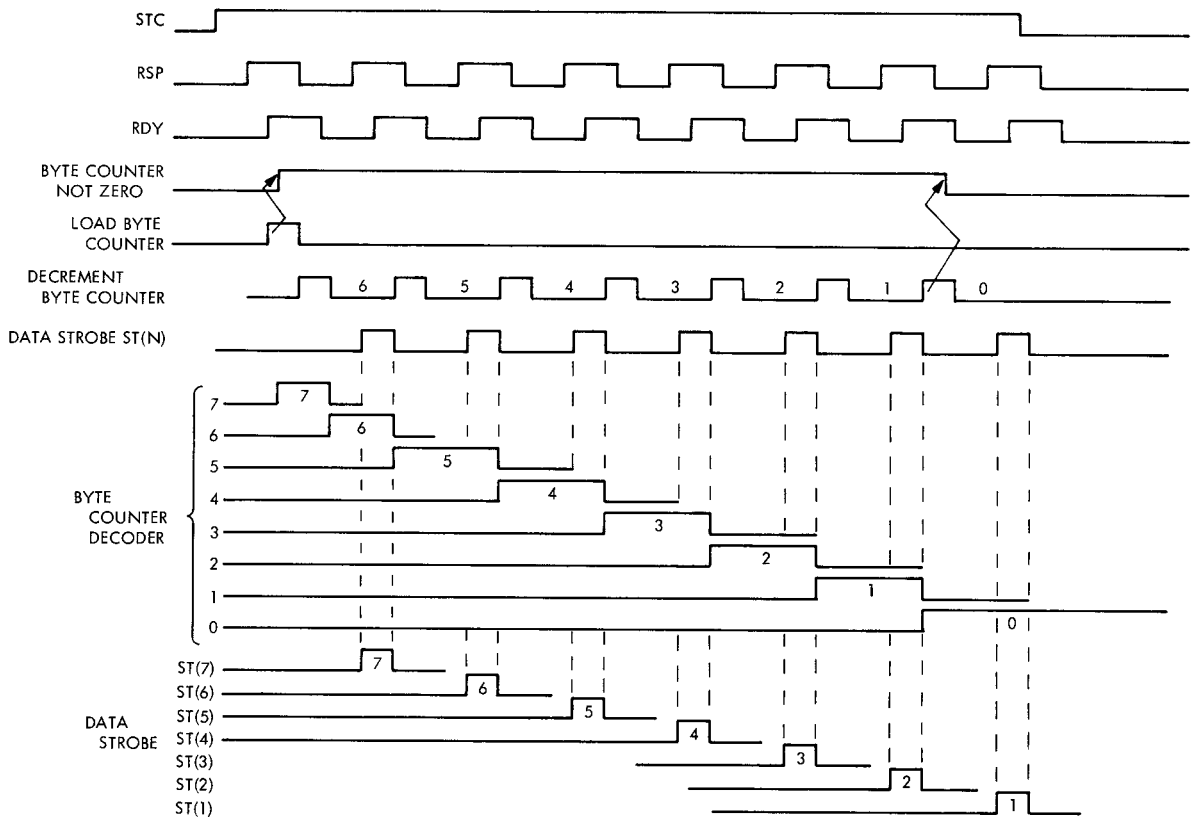

Fig. 11. Timing diagram for computer interface

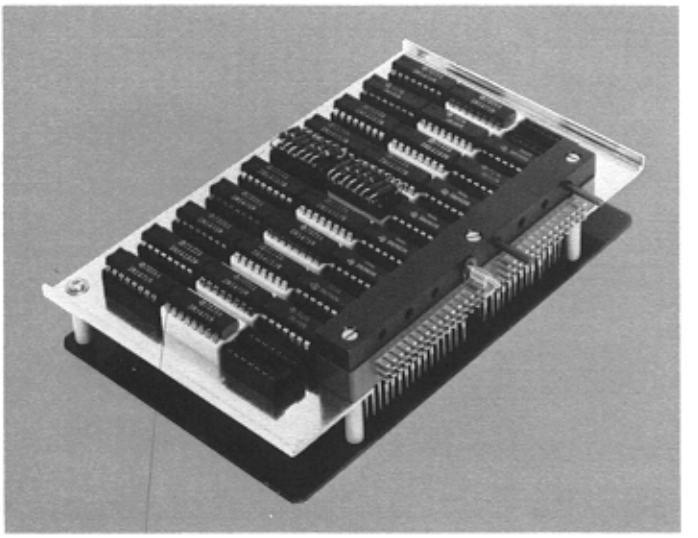

Fig. 12. Digital control plug-in card