Block IV Receiver Development

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This article describes a digital control assembly developed for use in controlling the frequency of a Dana Laboratory Digiphase synthesizer, Model 7010-S-179. The control assembly allows the synthesizer to be used as the oscillator within a phase-locked loop. A brief analysis using the synthesizer control assembly in a third-order loop is included.

I. Introduction

In the original Block IV analog loop design (Ref. 1), a crystal voltage-controlled oscillator (VCO) is combined with a programmed oscillator to provide both frequency agility and the capability of programming the local oscillator frequency to track the doppler. The programmed oscillator used in Block IV contains a Dana Laboratory Digiphase synthesizer (Ref. 2), essentially a number-controlled oscillator that can readily be adapted to function as a loop-controlled oscillator. This can be accomplished by digitizing the loop error signal and processing this digital information to control the synthesizer. In such a configuration, the VCO is eliminated and the frequency tracking range is no longer limited by the VCO frequency range. There are the added advantages of: (1) eliminating crystal oscillator drifts that offset the local oscillator frequency during acquisition, and (2) eliminating the need to combine two signals (VCO and synthesizer), which inherently introduces unwanted intermodulation products.

The type of loop design that would be most effective in tracking future spacecraft is being investigated. The use of a synthesizer as the loop-controlled oscillator still leaves open the option of using either a second- or third-order loop or modifications of these designs. Until now, the doppler rates and accelerations of spacecraft were not significant. Recently, however, during the extended-mission phase of the *Mariner* Mars 1971 mission, these rates became factors at low signal levels and exceeded the tracking capability of the second-order loop being used. In future probes, these rates will increase and become more significant at stronger signal levels, which will result in excessive tracking errors in second-order ground receivers. For this reason, a third-order loop using the synthesizer as the loop-controlled oscillator is being investigated to provide tracking capability without the need to program the synthesizer.

II. Loop Design

As mentioned previously, in the present Block IV receiver, the output from the Dana synthesizer is combined with a VCO to yield a sum frequency, which is subsequently multiplied to generate the local oscillator. The VCO is controlled by the loop and is used to track the phase of the received signal, while the synthesizer is used for automatically sweeping the local oscillator around the

received signal (for signal acquisition purposes) and for tracking the doppler of the received signal. To control the synthesizer in this configuration, a Programmed Oscillator Control Assembly (POCA) is used (Ref. 2).

To utilize the synthesizer as a loop-controlled oscillator, it is necessary to convert the loop phase error into the format required to control the synthesizer. This is done in the Receiver Loop Phase Control Assembly (RLPCA). The RLPCA is an extension of the POCA (Fig. 1), incrementing or decrementing the input to the synthesizer from the POCA. Designing the RLPCA to generate a synthesizer output frequency rate proportional to the polarity and magnitude of the loop phase error provides a third-order loop. Third-order loops in sensitive phase-lock receivers have been extensively analyzed (Ref. 3). In the following, the designs of both the RLPCA and the third-order loop for this application are presented.

III. RLPCA Design

Figure 2 is a simplified block diagram of the RLPCA. The receiver static-phase-error voltage is applied to the input of an absolute-value-plus-sign (AVS) module. The AVS module produces a unipolar output voltage proportional to a bipolar input and also a logic level (sign bit) to denote the input polarity. The need for the AVS module is predicated on the characteristics of the high-speed analog/digital (A/D) converter which it drives. The A/D converters available for this application accept unipolar voltages only.

The A/D converter driven by the AVS module provides a 12-bit binary output number proportional to the input voltage and can convert the analog voltage to this binary number in less than 4 μsec. This allows the input static phase error to be sampled each 100-kHz clock period and to complete the conversion during the first half-period of the clock. This is necessary because the Dana synthesizer samples the binary-coded decimal (BCD) input during the second half-period of the clock.

The binary number from the A/D converter is converted to a serial pulse rate by the pulse rate generator. This pulse rate is then proportional to the static-phase-error voltage. The pulses and the AVS sign bit (and its complement) are applied to the inputs of two logic gating circuits, G2 and G3. The gate circuit outputs are connected to the count up/down terminals on the least-significant (10^{-4}) BCD counter. When the receiver control functions are in the mode for the RLPCA to control the synthesizer frequency, the pulses generated by the pulse rate generator are coupled to the count up/down terminals of a BCD counter (10^{-4}-decade) through gate circuits G2 and G3. The sign bit supplied by the AVS module is also coupled to the inputs of G2 and G3, and it determines whether the pulses increment or decrement the number stored in the counter. The 10^{-4}-decade counter is cascaded with 11 similar BCD counters, which store the control numbers up to the 10^{7}-decade of the synthesizer. The BCD numbers at the counter outputs are fed directly to the synthesizer frequency control inputs.

Twelve BCD control numbers from the POCA are applied to the parallel inputs of the BCD counters. When the receiver status is such that the synthesizer is to be controlled by the POCA, the receiver status signal disables gates G2 and G3 and enables gate G1. Enabling G1 allows the BCD numbers from the POCA to be loaded into the up/down counters each clock cycle, and the counter output numbers then track the POCA. When the receiver status changes so that again the receiver phase is to be controlled by the RLPCA, gate circuit G1 is disabled and G2 and G3 are enabled. Thus, the number stored in the BCD counters is the last number supplied by the POCA plus or minus (depending on the AVS sign bit polarity) the accumulation of the pulses applied to the up/down counter terminals of the 10^{-4} decade. The synthesizer output frequency then varies at a rate proportional to the static-phase-error voltage.

The combination of the RLPCA and the Dana synthesizer (neglecting the numerical resolution of the A/D converter) has a frequency transfer function of

$$\frac{dw}{dt} = KE_i(t) \text{ rad/sec}^2 \tag{1}$$

where K is the sensitivity constant in rad/sec^2/V. In Laplace notation, Eq. (1) becomes

$$s^2\phi(s) = KE_i(s)$$

or

$$\phi(s) = \frac{KE_i(s)}{s^2} \tag{2}$$

IV. Third-Order Loop Design

A basic mathematical block diagram of the receiver loop is shown in Fig. 3. The design criteria for the receiver loop parameters adhere closely to those in Ref. 3 and some unpublished notes on cascade design of third-order loops by R. C. Tausworthe and R. B. Crow. Setting

$$G = AK$$

where A is the rms signal input voltage, and K is the total open-loop gain, the linear transfer function becomes

$$L(s) = \frac{G(\tau_2 s + 1)^2}{\tau_1 s^3 + (G\tau_2 + 1)s^2 + 2G\tau_2 s + G} \tag{3}$$

Setting

$$q = \frac{G\tau_2^3}{\tau_1}$$

Eq. (3) becomes

$$L(s) = \frac{q(\tau_2 s + 1)^2}{s^3 + \frac{q}{\tau_2}s^2 + \frac{2q}{\tau_2^2}s + \frac{q}{\tau_2^3}} \tag{4}$$

Testing the denominator of Eq. (4) for critical damping and solving for q,

$$q = 27/4 \text{ at critical damping} \tag{5}$$

Setting $s = j\omega$ in Eq. (4) and taking the squared absolute value,

$$|L(j\omega)|^2 = \frac{q^2(\tau_2^4\omega^4 + 2\tau_2\omega^2 + 1)}{\omega^6 + \frac{q}{\tau_2^2}(q-4)\omega^4 + \frac{2q^2}{\tau_2^4}\omega^2 + \frac{q^2}{\tau_2^6}} \tag{6}$$

Integration of Eq. (6) over all frequencies yields the loop noise bandwidth:

$$w_L = \frac{q}{2\tau_2}\left(\frac{2q+3}{2q-1}\right) \tag{7}$$

The loop parameters are selected such that the loop is never underdamped (pp. 9–12, Ref. 3). This is accomplished by letting the design point q in Eq. (5) be

$$q_0 = \frac{G_0\tau_2^3}{\tau_1} = 27/4 \tag{8}$$

where G_0 is the design point open-loop gain. The lead time constant τ_2 then is derived from Eq. (7) by

$$w_{L,0} = \frac{q_0}{2\tau_2}\left(\frac{2q_0+3}{2q_0-1}\right) = \frac{4.455}{\tau_2}\text{ Hz} \tag{9}$$

or

$$\tau_2 = \frac{4.455}{w_{L0}}\text{ sec}$$

Tracking errors due to input phase transients, $\phi_i(s)$, can be calculated by

$$\epsilon\phi(s) = \phi_i(s)[1 - L(s)] \tag{10}$$

and the steady-state tracking error, ϕ_{ss}, by

$$\phi_{ss} = \lim_{s\to 0} s\phi_i(s)[1 - L(s)] \tag{11}$$

The $1 - L(s)$ term in Eq. (11) is obtained from Eq. (3):

$$1 - L(s) = \frac{\tau_1 s^3 + s^2}{\tau_1 s^3 + (G\tau_2^2 + 1)s^2 + 2G\tau_2 s + G} \tag{12}$$

The steady-state tracking error due to an initial offset phase ϕ_0, an initial offset frequency $\Omega_0 t$, and a doppler rate $\Lambda_0 t^2/2$ is calculated by Eqs. (11) and (12):

$$\phi_{ss} = \lim_{s\to 0} \frac{\left(\frac{\phi_0}{s} + \frac{\Omega_0}{s^2} + \frac{\Lambda_0}{s^3}\right)s^3(\tau_1 s + 1)}{\tau_1 s^3 + (G\tau_2^2 + 1)s^2 + 2G\tau_2 s + G} \tag{13}$$

$$\phi_{ss} = \frac{\Lambda_0}{G}\text{ rad} \tag{14}$$

To calculate the value of τ_1, Eq. (8) is solved for G_0 and substituted in Eq. (14):

$$\phi_{ss} = \frac{\Lambda_0}{G_0} = \frac{\Lambda_0\tau_2^3}{\tau_1 q_0}$$

from which

$$\tau_1 = \frac{\tau_2^3 G_0}{q_0}\text{ sec} \tag{15}$$

A typical design example would be as follows:

$$\begin{aligned} G_0 &= K_D G_A K_V K_M \times 360\alpha_0 \\ &= \frac{5}{57.3}\ \text{(V/deg)} \times 100\ \text{(V/V)} \\ &\quad \times 2\ \text{(Hz/sec/V)} \times 40 \times 360 \times 0.06 \\ &= 1.5079 \times 10^4 \end{aligned}$$

$$w_{L0} = 3\text{ Hz}$$

$$\Lambda_0 = 200\text{ Hz/sec at S-band}$$

$$\tau_2 = \frac{4.455}{3} = 1.485\text{ sec (from Eq. 10)}$$

$$\tau_1 = \frac{(1.485)^3 \times 1.5079 \times 10^4}{6.75} = 7.316 \times 10^3\text{ sec (from Eq. 15)}$$

$$\phi_{ss} = \frac{360 \times 200}{1.5079 \times 10^4} = 4.4775\text{ deg (from Eq. 14)}$$

V. Concluding Remarks

The circuit design of the Receiver Loop Phase Control Assembly has been accomplished, and a breadboard model of the circuit is currently under construction. The design will be evaluated in the engineering model of the Block IV receiver.

References

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3. Tausworthe, R. C., "Practical Design of Third-Order Phase-Locked Loops," Report 900-450, Apr. 27, 1971 (JPL internal document).

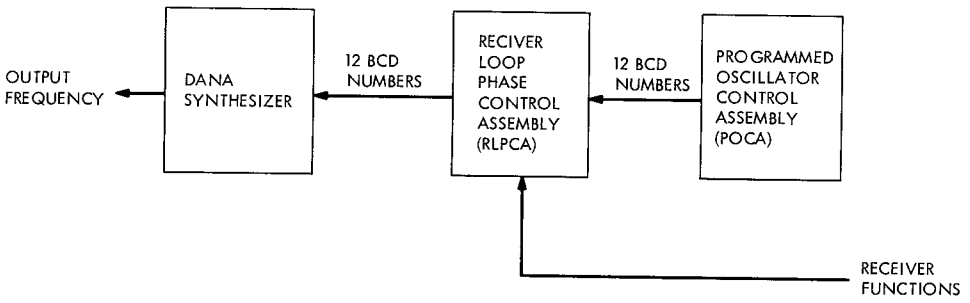

Fig. 1. Receiver Loop Phase Control Assembly application

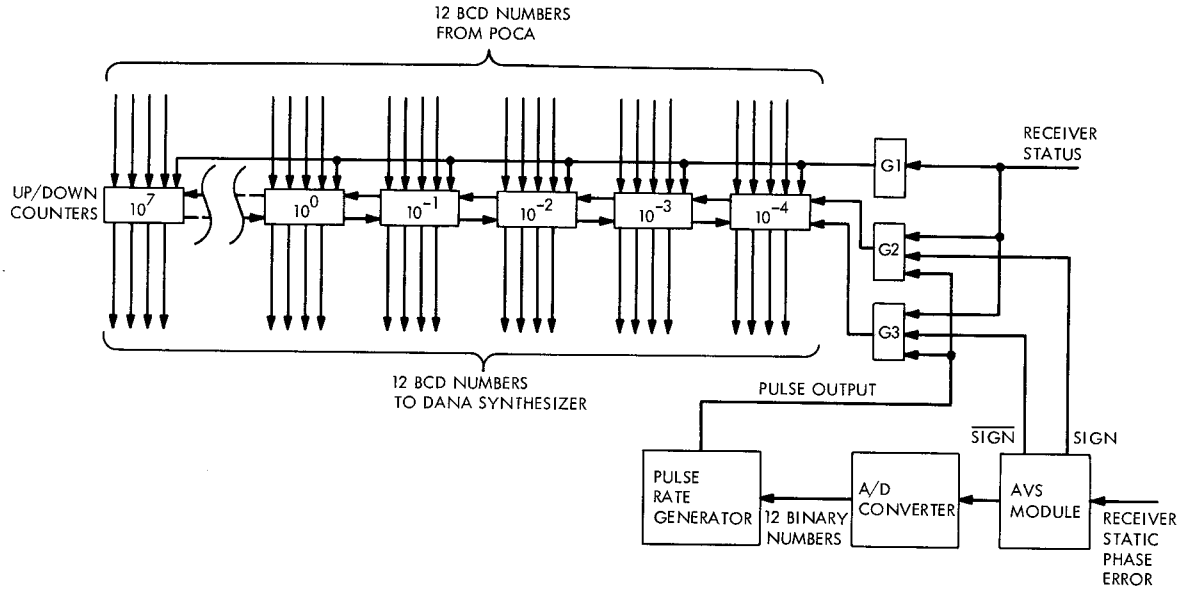

Fig. 2. Block diagram of Receiver Loop Phase Control Assembly

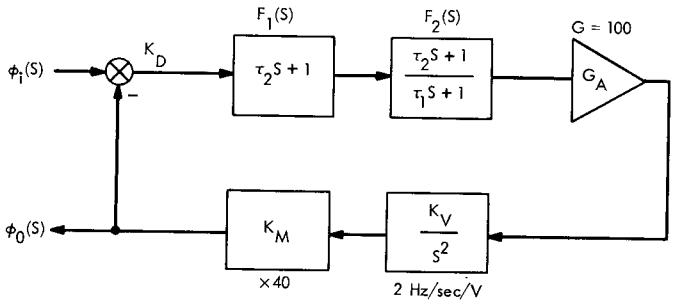

Fig. 3. Receiver loop block diagram