L-Band Frequency Multipliers: Phase Noise, Stability, and Group Delay

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In this article, three 100- to 1400-MHz frequency multipliers are evaluated for use in the hydrogen maser receiver–synthesizer, with the conclusion that significant advancements have been made in the design of step recovery diode multipliers. In addition, while it appears that the group delay performance in multipliers can be quite good, there are substantial problems that prevent resolving group delays of <1 nsec in frequency multipliers.

I. Introduction

Three different types of ×14 frequency multipliers were tested. First, a discrete-component frequency multiplier was built using Schottky barrier diodes as the only non-linear elements in an attempt to achieve the lowest possible phase noise. Next, Zeta Laboratories, which claims to have made important advancements in multiplier design, supplied two ×14 multipliers to JPL for evaluation and testing. Finally, a unit which typifies conventional step-recovery-diode multiplier design was obtained from Frequency Sources, Inc. as a second source in procurement specifications.

II. Construction and Design of the Multipliers

The JPL ×14 multiplier[1] uses commercial modular components assembled on an aluminum plate and interconnected with semi-rigid coax. The only adjustments required are the insertion of attenuators in the lines to set the power levels.

The Zeta multiplier is unusual in that it employs a sampling phase-locked loop to reference a 1400-MHz strip-line voltage-controlled oscillator (VCO) to the input. This technique has the advantage of holding the output power level constant, independent of level or frequency, but it requires a VCO with good phase noise characteristics. The unit is quite complex, utilizing a strip line and two printed circuit boards incorporating a total of ten transistors and two integrated circuits. However, there are only two RF adjustments plus a trimpot, which adjusts a digital searching circuit that sweeps the VCO to acquire lock. An isolator is required at the output to prevent pulling of the VCO and erratic phase lock.

The Frequency Sources ×14 multiplier typifies the present design of step-recovery-diode multipliers by

[1]Described in detail in Ref. 1.

incorporating a high-powered two-transistor amplifier with many tuning adjustments in addition to a three-stub tuner on the output. Although the circuit design is relatively simple, the numerous tuning adjustments result in a complex alignment procedure and a rather narrow bandwidth.

III. General Performance

Table 1 gives a direct comparison of these three very different multipliers over a wide variety of parameters. The cost of the JPL $\times 14$ multiplier (basic parts, no packaging) is approximately four times that of the other units. The JPL $\times 14$ multiplier's output level and bandwidth are the most sensitive to the input level due to the numerous doublers and filters; however, the absence of high-Q circuits provides a much wider bandwidth compared to that of the other multipliers. The output level of the Frequency Sources multiplier remains relatively constant over a wide range of input power, which probably indicates a good matching network that keeps the step recovery diode well saturated. However, the high-Q circuits tend to narrow the bandwidth and allow the center frequency to shift nearly 3 MHz over a 0–50°C temperature range. The Zeta multiplier's output is perfectly flat since the VCO requires only an input signal greater than -3 dBmW in order to acquire lock. Although 13 MHz is the bandwidth in which the Zeta multiplier will reliably acquire lock, the actual information capacity of the multiplier is very low since the phase modulation capability is limited by a loop bandwidth of only 2.6 kHz.

IV. Stability

Instability is caused when a phase drift rate (equivalent to a frequency offset) is generated by a change in temperature. To compare the multipliers, a 5°C step change in temperature was arbitrarily assigned as a worst-case situation, and the maximum rates of change in phase were subsequently recorded. Since the stability depends only on the rate of change in the phase, and not the absolute change, the thermal isolation of the module affects greatly the degree of stability actually attained. However, un-isolated measurements are meaningful in that it has been determined that, when a device is mounted inside a module and then placed in a rack as part of a system, a factor-of-10 improvement over the free air stability can be expected. However, to obtain improvement factors of 100 or 1000, special insulation or ovens are definitely required. The three multipliers are judged about equal in stability when operating as part of a packaged system. The JPL $\times 14$ multiplier exhibited a poorer stability because its tubular filters were exposed to the oven's air blast without benefit of any thermal shielding. It should also be emphasized that, since the measured free air stability depends largely on the magnitude of the temperature change selected for the test (i.e., the temperature coefficient of phase is not constant), the temperature step should be the same as the actual variation expected in the system environment.

V. Phase Noise

The power spectral density of phase noise for the Zeta multiplier is equal to the noise of the JPL $\times 14$ and is 12 db lower than that of the Frequency Sources multiplier. Apparently, Zeta actually has made advances in the design of step-recovery-diode multipliers. From the research performed so far, the improvement in phase noise is the most likely due to a reduction in the overall positive feedback present in the multiplier circuit. The fact that the step recovery diode is a one-port device exhibiting a negative resistance characteristic has always placed severe constraints on the circuit design, in which the objective is to eliminate parametric instabilities while simultaneously maximizing efficiency and bandwidth. In the Zeta multiplier, the step recovery diode only pulses the sampling gate and therefore eliminates the customary filtering and idling circuits required.

VI. Group Delay

Group delay is defined as the time required for information to pass through a system. Alternatively, group delay can be viewed as $d\phi/d\omega$, where ϕ, in rad, is the phase shift through the system, and ω is the input frequency in rad/sec. These two interpretations of group delay suggest two methods of measurement.

For simplicity, first consider the case of a system where the input and output frequencies are the same. Figure 1a depicts an arrangement that measures $\Delta\phi/\Delta\omega$ by shifting the frequency an amount $\Delta\omega$ and then recording the resultant change of phase. The process is then repeated over the desired range of frequencies.

Figure 1b is a second method for determining group delay that essentially measures the time required for modulation to pass through the system. Here, the signal source is amplitude-modulated by a modulating frequency and then detected after passing through the sys-

tem under test. By comparing the phase of the modulated and detected signals, the group delay is simply:

$$t_d = \frac{\phi}{360 f_m}$$

where

t_d = group delay, sec

ϕ = phase shift, deg

f_m = modulating frequency, Hz

Obviously, to avoid ambiguities in the above equation, the group delay must be less than the period of the modulating frequency. In addition, the delays of the modulator and detector must be subtracted from the measured delay to obtain the absolute delay of the device under test. In a system, since it is usually sufficient to know only the *change*[2] in group delay as a function of various parameters, it is not necessary to calibrate the absolute delays of the modulator and detector. Although the resolution of this system improves as the modulating frequency increases, it is important that the frequency of modulation remain small with respect to the bandwidth of the device under test to insure that the carrier and both sidebands see approximately the same transfer function.

Measuring the group delay of frequency multipliers or dividers with the techniques of Fig. 1 will not succeed, because the input and output frequencies are no longer the same. The system of Fig. 2a resolves this difficulty by creating a reference channel with a second device. Group delay is measured as in Fig. 1b, except that phase modulation must be used since amplitude modulation will not pass undistorted through the usual type of multiplier or divider. Often, the group delay of the modulator is a function of the source frequency; so, to prevent error, the modulation frequency is detected prior to entering the device under test by means of a second phase detector (Fig. 2b). The phase detector consists of a double-balanced mixer with the input signals supplied in quadrature by a variable phase shifter. Since the phase detector is a symmetric device reading the phase difference between two channels, its effect on the group delay is negligible, provided the S-curve is linear. Any nonlinearity present in which the phase detection slope becomes a function of the operating point can easily be observed by varying the phase shifters and noting any change in the phase meter reading.

The group delay of the JPL $\times 14$ multiplier was measured with the system of Fig. 3, using a modulation frequency of 2.777 MHz. This frequency is well within the bandwidth of the multiplier and allows a conversion of 1 nsec/deg of phase. Since the modulation index must be kept low in order that there be only one pair of sidebands after $\times 14$ multiplication, the detected signal at the reference point A is too small for the vector voltmeter to lock onto it. Therefore, the reference for the vector voltmeter must be taken directly from the 2.777-MHz source and then the results corrected for the group delay characteristic of the phase modulator. This is accomplished by recording the group delay response in the "calibrate" position of Fig. 3 and then subtracting it from the final results.

The resolution of this test system is about 0.1 nsec; however, after many runs to verify repeatability, it was determined that there is an overall uncertainty of about ± 0.5 nsec in the data. This is attributed to the fact that certain delays in the system, especially in the phase modulator, are very sensitive to signal level. Figure 4 shows the variation in group delay for only the discrete $\times 14$ multiplier, since the bandwidths of the other multipliers were too narrow to use a high enough modulation frequency for adequate resolution.

[2]Group delay distortion arises when the spectral components of a complex waveform are delayed unequally during transmission, because the group delay of a device is a function of frequency. Thus, in most systems it is the variation of the group delay with frequency, temperature, or power supply voltage that results in distortion or timing errors.

Reference

1. Lutes, G., MacConnell, J., and Meyer, R., "Hydrogen Maser: Low Phase Noise, L-Band Frequency Multiplier," in *The Deep Space Network Progress Report for November and December 1971*, Technical Report 32-1526, Vol. VII, pp. 81–83, Jet Propulsion Laboratory, Pasadena, Calif., Feb. 15, 1972.

Table 1. Comparison of frequency multipliers

Parameter	JPL ×14	Zeta	Frequency sources	Unit
Output power @ 13-dBmW input	17.0	17.2	17.4	dBmW
1-dB output bandwidth @ 13-dBmW input	28	13[a]	3.7	MHz
Spurious level	>60	>60	>60	dB down
Power spectral density of phase noise[b] @ 10 Hz	−110 dB	−110 dB	−98 dB	rad²/Hz
Phase noise[c] @ 10 Hz	180	180	730	μdeg rms/Hz½
Phase drift	4.1	3.7	3.7	deg/°C
Phase drift rate for a 5°C step change in temperature	90	27	18	mdeg/sec
Stability for a 5°C step change in temperature	18	5.4	3.6	parts/10^{14}
Change in output power over 0–50°C	4	1	1.5	dB
Change in output power for a 6-dB change in input level	4	0	0.8	dB
Change in output power for a 20% change in power supply voltage	1	1	0.5	dB
Change in bandwidth over 0–50°C	4	—	2	MHz
Change in bandwidth for a 6-dB change in input level	20	0	0.2[d]	MHz
Change in group delay for a 10°C change in temperature	1	—	—	nsec
Bandwidth for a 1-nsec variation in group delay	11.2	—	—	MHz
Number of RF tuning adjustments	0	2	16	—
Number of transistors and integrated circuits	14[e]	12	2	—
DC power required	24 V @ 320 mA 15 V @ 75 mA 12 V @ 55 mA	28 V @ 200 mA	28 V @ 200 mA	—
Size	41 × 33 × 5 (16 × 13 × 2)	10 × 10 × 5 (4 × 4 × 2)	15 × 6 × 4 (6 × 2.5 × 1.5)	cm (in.)

[a]Multiplier utilizes a phase-locked loop that will reliably acquire lock within a 13-MHz bandwidth.
[b]System noise: −145 dB rad²/Hz.
[c]System noise: 3.2 μdeg rms/Hz½.
[d]Center frequency of the bandwidth shifts about ±1.3 MHz for a ∓25°C change in temperature.
[e]Number of modular components.

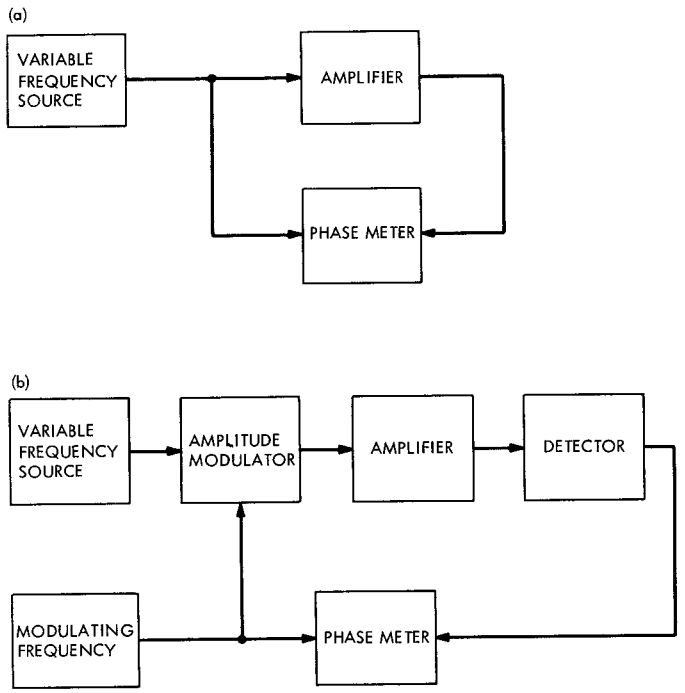

Fig. 1. Group delay measurement of amplifiers

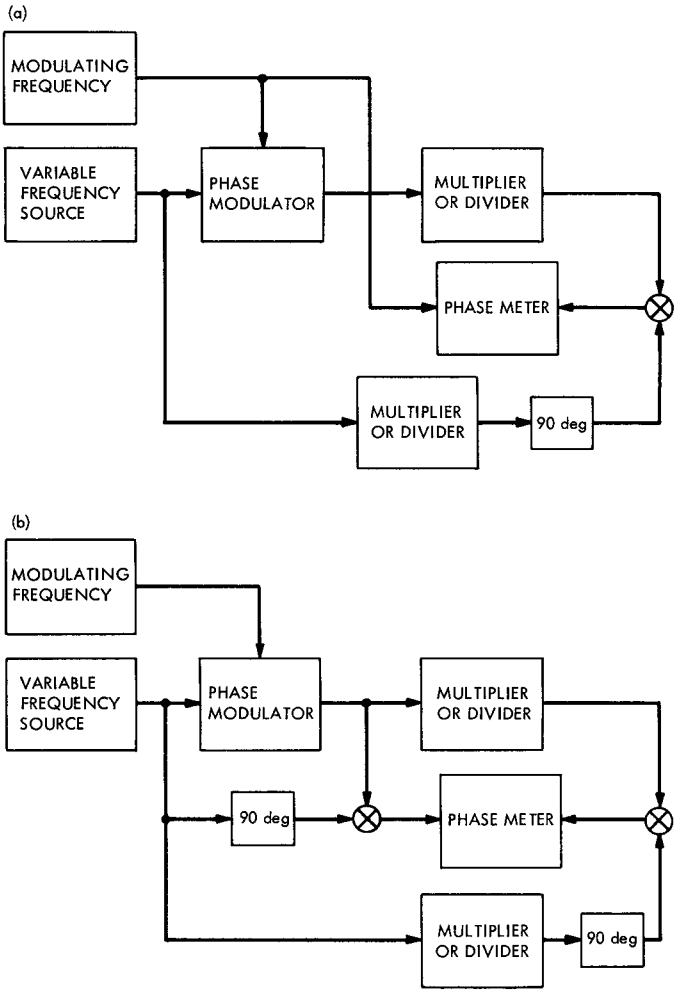

Fig. 2. Group delay measurement of multipliers and dividers

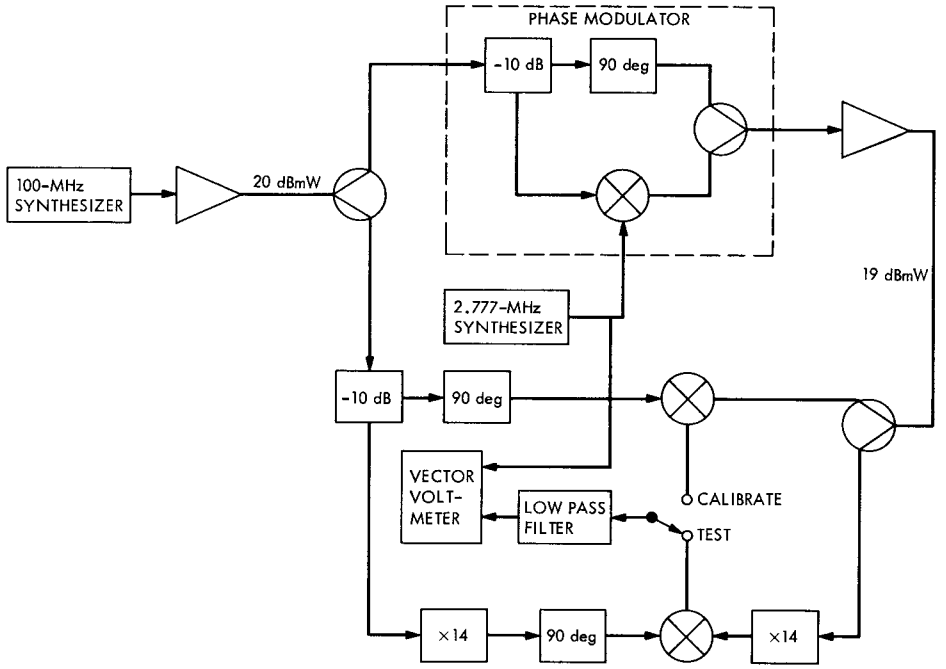

Fig. 3. Group delay measurement of ×14 multiplier

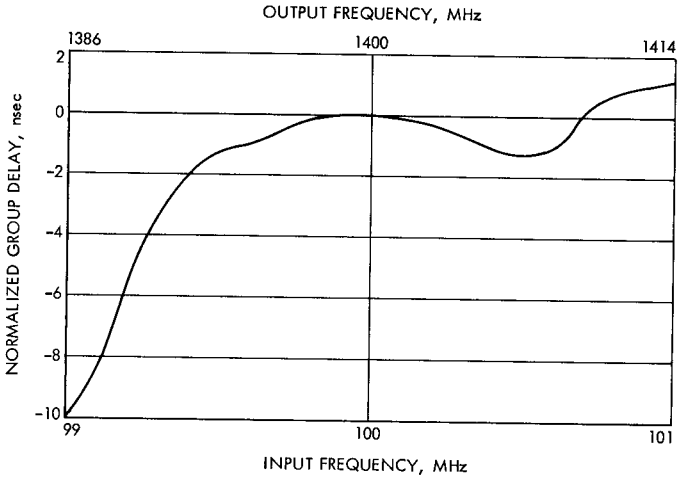

Fig. 4. Normalized group delay of the JPL ×14 multiplier