Digital Frequency Shifter

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Digital techniques applied to the development of frequency shifters yield a circuit that exhibits both wide bandwidth and exceptionally low phase noise while requiring no alignment.

I. Introduction

Phase-coherent frequency shifters are employed within the Block IV receiver/exciter to generate reference frequencies that are coherently related to the exciter oscillator frequency by factors of 912/221 and 2636/221 (Fig. 1). These reference frequencies are used both in the S- and X-band doppler extractors and coherent translators. Previously developed frequency shifters for the Block III receiver/exciter utilized parametric devices or locked oscillators to accomplish the frequency division process of the shifters (Refs. 1, 2). These methods of frequency division exhibit narrow bandwidth because of the use of tuned elements, high phase noise, and extensive alignment time because of their rigorous alignment procedure.

To eliminate the disadvantages of present frequency dividers and also provide the increased frequency range required for the Block IV receiver/exciter, high-speed synchronous digital counters are being used as the frequency division elements. This article describes the application of these counters.

II. Design

The frequency shifters utilize a family of emitter coupled logic elements (ECL) that exhibit sub-nanosecond switching times and the ability to clock at frequencies in excess of 100 MHz. The fast switching characteristics keep the phase noise and phase drift vs. temperature ratio low.

Basic to the operation of the frequency shifters are two high-speed synchronous counters having modulos of 13 and 17. Figure 2, a block diagram of the 912/221 frequency shifter, illustrates the relative location of these high-speed counters within the frequency shifter. The counters are used to generate signals with the prime frequency ratios of 13/221 (1/17) and 17/221 (1/13). These signals are then multiplied by 7 and differenced to provide an output signal related to the input by the frequency ratio of 28/221.

Figure 3 is a functional diagram of the 28/221 synthesizer section of the frequency shifter illustrating the logical implementation of the counters. The logical variables in the counter feedback loops were selected to provide output rectangular waveforms that are related to the 43-MHz input carrier by factors of 17/221 and 13/221 and yield large harmonic content in the output waveforms. The counter output waveforms are then presented to bandpass filters that select the power in the 7th harmonic and reject the power in all other spectral lines. This frequency selection effectively provides the $\times 7$ multiplication functions and generates frequencies

related to the input carrier by factors of 91/221 and 119/221. These frequencies are amplified and applied to the inputs of a balanced mixer, where a difference frequency of 28/221 relative to the input carrier is produced. The remainder of the synthesis is accomplished using a method of frequency addition and selection.

III. Performance

Phase noise and phase delay vs. temperature tests have been performed on components of the 28/221 synthesizer. Figure 4a shows a phase noise performance setup for modulo 13 and 17 counters. The counter/multiplier was compared against an identical reference assembly. The two assemblies were driven by the same signal to eliminate the noise of the source. The comparison is made in a balanced mixer configured as a phase detector. The measurement results are shown in Fig. 4b, an oscilloscope presentation of the phase detector output. The broad baseline is setup noise, and the slight perturbations are phase noise, indicating a phase noise output of less than 0.004 deg P-P.

Phase delay vs. temperature effects were plotted using the measurement setup shown in Fig. 5. The reference channel was maintained at room ambient temperature. The assembly under test was cycled between 0 and 50°C in 5°C increments. The delay varied a total of 6 deg monotonically between the temperature extremes of 0 and 50°C for a phase shift of 0.12 deg/°C.

IV. Conclusions

Digital techniques have been successfully employed to produce RF frequency shifters that exhibit exceptional phase noise and phase delay vs. temperature characteristics, are broadband, and require no alignment except for a control to set the output power level.

References

1. Johns, C. E., "5/221 Parametric Frequency Divider," in *The Deep Space Network*, Space Programs Summary 37-22, Vol. III, pp. 7–9, Jet Propulsion Laboratory, Pasadena, Calif., July 31, 1963.
2. Johns, C. E., "57/221 Frequency Shifter—Block IIB," in *The Deep Space Network*, Space Programs Summary 37-42, Vol. III, pp. 83–86, Jet Propulsion Laboratory, Pasadena, Calif., Nov. 30, 1966.

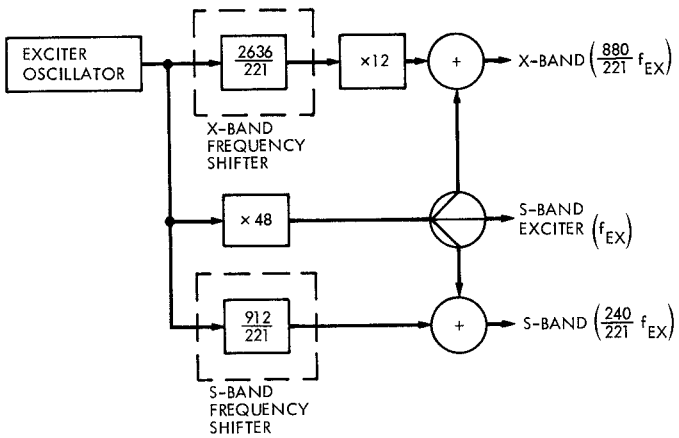

Fig. 1. Block IV frequency shifters

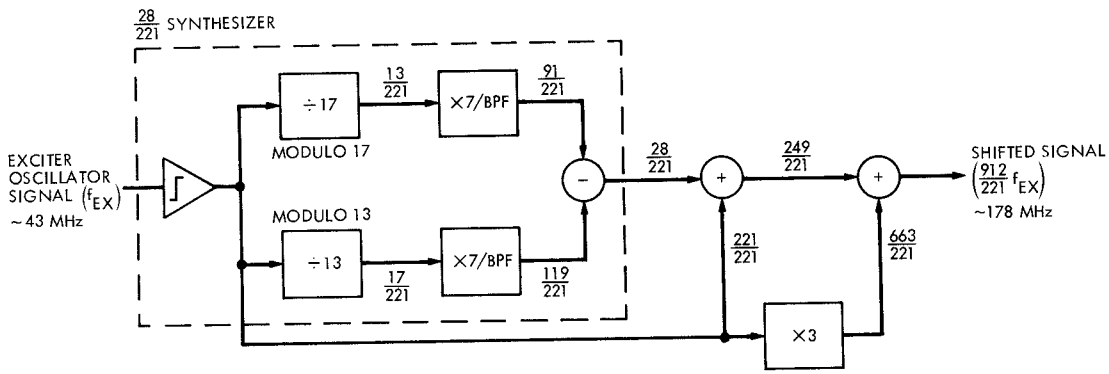

Fig. 2. 912/221 frequency shifter

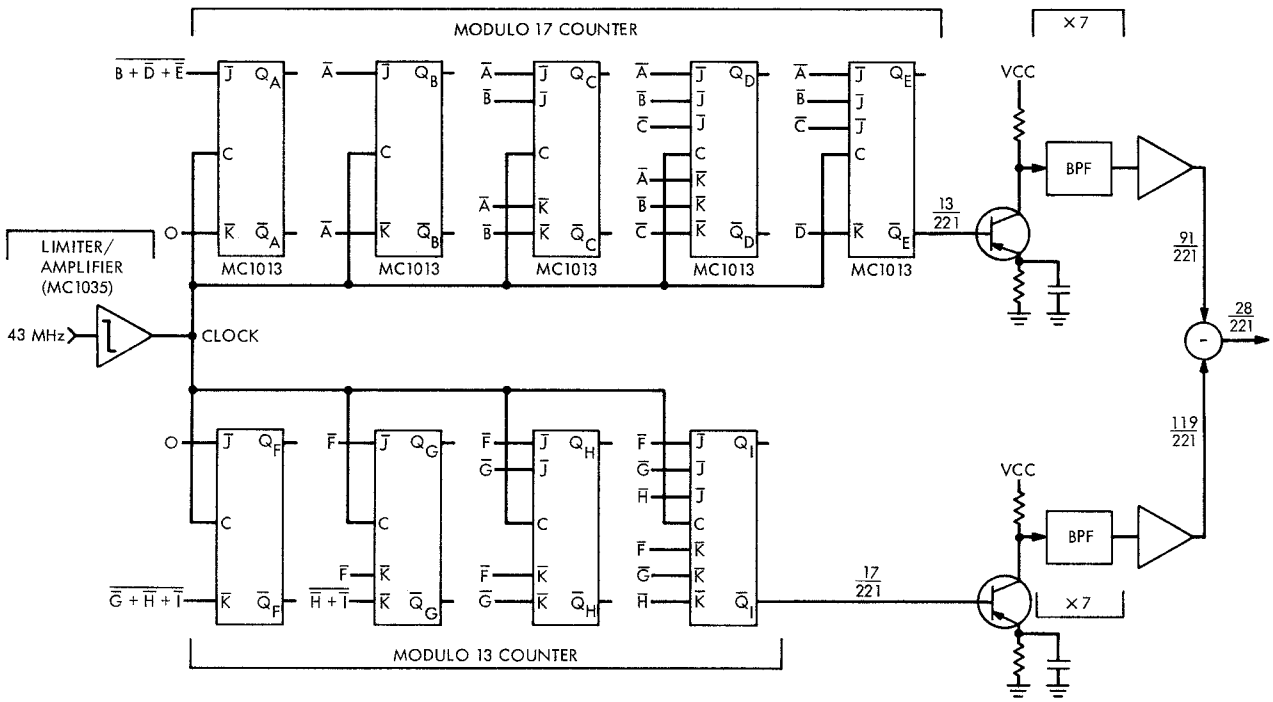

Fig. 3. 28/221 frequency synthesizer

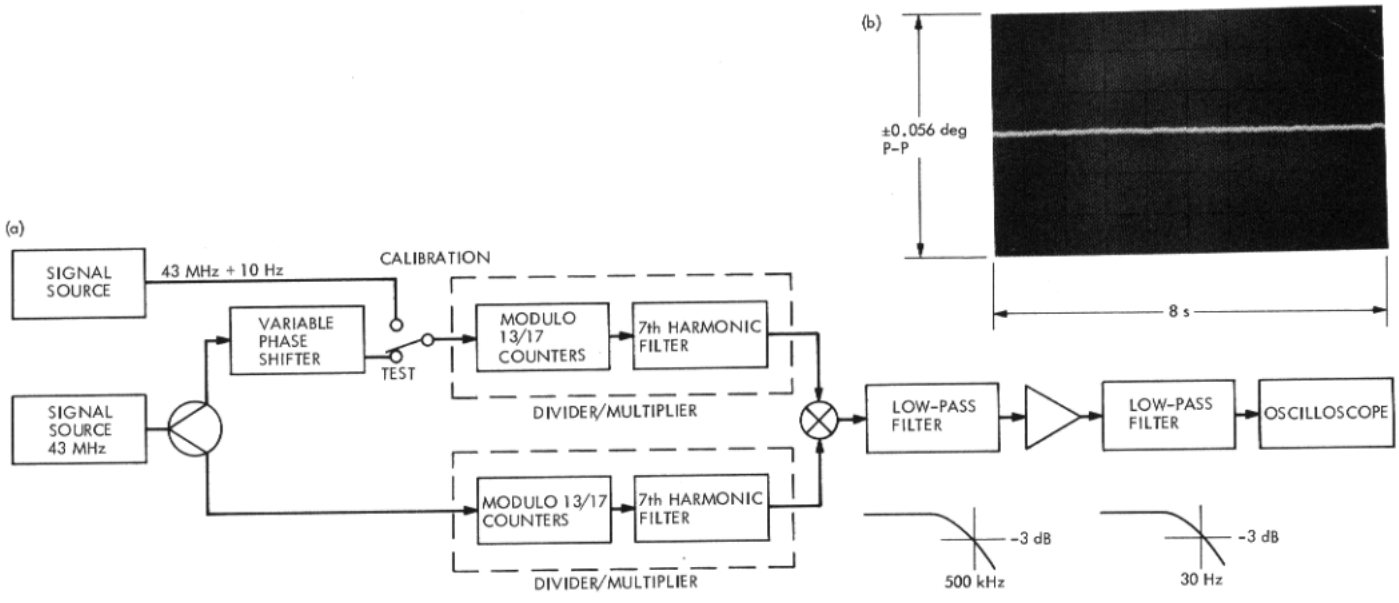

Fig. 4. Phase noise measurement

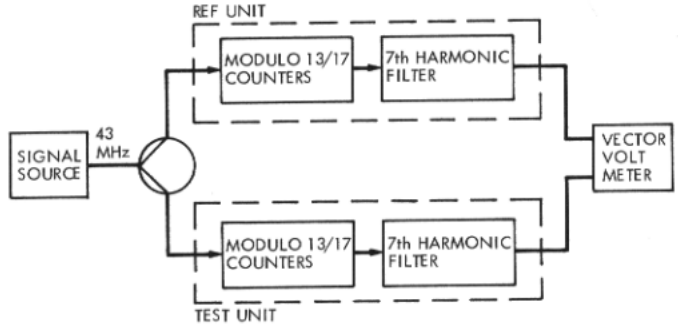

Fig. 5. Phase delay stability measurement