Two-Station Interferometer Analog Input Channel

T. O. Anderson
Communications Systems Research Section

A signal sampling system, used for the Deep Space Network Venus two-station radar experiment, intended to demonstrate hydrogen maser compatibility in two-station spacecraft tracking with planetary round trip times, has been implemented. One sampling channel is described in detail. Four such channels, one for the sine and one for the cosine signal from each of two antennas, are used in the demonstration interferometer system. Each channel contains two multiplexed subchannels, and each subchannel consists of an integrating circuit, a track-and-hold circuit, and an analog-to-digital converter. All components of the subchannels are multiplexed and the output is derived from a digital multiplexing circuit which puts out digital data in parallel to line drivers for computer connection. Part of the four-channel system, a special-purpose test and calibration system, is also described.

I. Introduction

Analysis (Ref. 1) indicates that by properly processing the simultaneous two-way doppler and range data from two stations, the errors resulting from low-declination geometry of outer planet spacecraft are reduced by a factor of 2 to 4, and the errors resulting from unmodeled spacecraft accelerations are reduced by 2 orders of magnitude. To demonstrate the feasibility of maintaining phase coherence between two stations, one transmitting and both receiving, and each with its own hydrogen maser frequency standard, a Venus interferometer radar experiment was conducted during June 1972. The experiment consisted of transmitting 400 kW from DSS 14, and after a round trip delay to the planet Venus of 5–10 min, simultaneous reception at DSS 14 and at DSS 13. The IF signal from DSS 14 was sent over a microwave link to DSS 13, where both signals were digitally processed. The equipment used to convert the receiver output analog signals into digital form for the demodulators and subsequent range-gated spectrum analysis is described in this article.

The analog input channel has parallel integrate-and-dump, sample-and-hold, and analog-to-digital conversion circuits. The outputs of the parallel A/D converters are digitally multiplexed onto a single line to the demodulator/filter unit. Parallel channels are required to allow continuous sampling with integrate-and-dump circuits which require approximately 1 μs to dump. The integrate-and-

dump circuits are used as a matched filter for rectangular pulses. Although this equipment was constructed primarily for radar data acquisition, the basic design is compatible with any DSN system using rectangular pulses, such as command, telemetry, and, especially, ranging.

In planning a system such as that described here, one is faced with a make-or-buy decision. Considering the large number of complete lines of digital data handling systems modules presently available in the market place, this decision becomes a selection of the optimum price/performance, yet compatible systems modules. Some additional special-purpose input/output and control circuits are also required. The only circuit for which the buy-or-make decision presented a question was the integrate-and-hold circuit. No single circuit module which would be usable for integration and subsequent holding and would also be sufficiently fast appeared to be available. Single integrate-and-reset circuits with sufficient speed and single track-and-hold circuits of sufficient speed are indeed available, however.

Other system configurations such as analog multiplexing of integrators with a single hold circuit and an A/D converter have been considered. Speed and accuracy appear to be limiting factors in analog multiplexing schemes. So-called tracking A/D converters have also been considered where the digital value of the integrator output signal may instantaneously be transferred to a hold register at any arbitrary time. No hold circuits would then be required. Tracking converters, however, are usually of lower resolution and are also high priced.

The configuration of the present system is shown in block diagram form in Fig. 1.

II. Integrate and Reset Circuit Module

Burr-Brown's sample-and-hold amplifier model 4013-2/25 is connected to operate as a switched integrator. Its block diagram is shown in Fig. 2. It includes a high-gain, wide-bandwidth field effect transistor (FET) input operational amplifier and a high-gain current output amplifier. It resets from ± 5 V to 0 ± 1 mV in less than 1 μs. The 4013-2/25 model includes a 0.001 $\pm 1\%$ μf polystyrene capacitor. The integrating resistor, which must not be smaller than 500 Ω, is connected externally. The 4013-2/25 model also has facility for external connection of a 2-kΩ potentiometer to provide a variable bias for the operational amplifier input offset voltage over a ± 10-mV range. The switched current amplifier is controlled by a transistor-transistor logic (TTL) compatible square wave derived from a high-speed flip-flop (FF).

III. Sample-and-Hold Circuit Module

The Analog Devices SHA-IIA, shown in block diagram form in Fig. 3, is used as the sample-and-hold circuit. Its accuracy and droop rate are compatible with a 12-bit resolution, 5-μs conversion time A/D converter. The accuracy is 0.01% of ± 5 V, to which it settles in 500 ns. The droop rate is 100 μV/μs, i.e., less than 0.1 least significant bit (LSB) of a 1-μs, 12-bit converter.

Confusion often exists between manufacturers' definitions of aperture time, acquisition time, and settling time. Figure 4 is a timing diagram defining these times. It also shows the specific times for the SHA-IIA. Other pertinent data on the SHA-IIA are: The input impedance is 10^{11} Ω. The output can supply 20 mA at ± 5 V. The settling time to 0.01% of ± 5 V or 5 mV accuracy is 500 ns maximum and for 0.1% of full scale (FS), the settling time is 300 ns. The full power frequency response in the track mode is 1.5 MHz.

The SHA-IIA has facility for connection of an external 100-Ω potentiometer for zero offset adjustment. This offset adjustment controls an internal compensation voltage and should be adjusted during the hold mode. During the *track* or *sample* mode there then remains a residual offset of a few millivolts which, however, is of no concern for the final output. Figure 5 is a chart showing the zero adjusted integrator output and the zero adjusted sample-and-hold amplifier output. The integrator input is assumed to be a DC voltage.

It was discovered that the SHA-IIA offset is critically sensitive to the switching speed of the digital control signal. The logic control signal is then derived directly from a high-speed FF.

IV. Analog-to-Digital Converter Module

The DATEL ADC-N10BC3 is used as the analog-to-digital converter. It converts the output from the sample and hold circuit to a 10-bit word in less than 4 μs. It is factory set for ± 5-V FS input. The output code is the 2's complement code shown in Fig. 6. The unit generates its own clock to supply a conversion rate of approximately 250 kHz. It requires a positive *start* convert pulse. It resets at the high level and starts to convert on the trailing edge. It responds with both a conversion-in-progress status signal and the bit conversion clock pulses. The unit has the facility for a 25-kΩ potentiometer for offset adjustment and a 100-Ω potentiometer for gain adjustment. The offset and gain adjustments are not entirely independent.

V. Output Digital Demultiplexing Circuit

Shown in Fig. 7 is the output demultiplexer implemented with wired OR line driving NAND-gates.

There are two output connections for each channel—one for the digital demodulator and one for the test system. The output to the test system is isolated from the demodulator output through a set of inverting buffers. The same digital control signal that controls the integration and sample-and-hold circuit also controls the output demultiplexer.

VI. Timing Control Unit

The input to the timing control unit shown in Fig. 8 is an auxiliary clock signal in the form of a 200-ns-wide negative pulse from +5 V to ground appearing at intervals no shorter than 5 μs. The clock signal is received by an inverting amplifier and is used to trigger an edge-triggered high-speed FF. The output from this FF controls the integrators, the sample-and-hold circuits, and the digital demultiplexer. The input clock pulse is AND-ed with the FF outputs to form the A/D converter *begin-conversion* pulses.

VII. Test System

The test system contains a five-position 10-bit multiplexer. Each channel may be manually selected, or all channels may be scanned at high speed. The test system also contains a test channel which consists of a set of 10-bit switches. The output from the multiplexer drives a 12-bit de-glitch D/A converter whose output may be biased $\pm$5 V for high-gain scope studies of $\pm$FS. The test system also contains a clock pulse simulator.

VIII. Clock Simulator

Figure 9 is a block diagram of the clock simulator. Cascaded programmable 4-bit binary ripple counters are used. These counters are used only as dividers and are connected to count between two vectors selected for convenient detection and set operation. This connection of the pulse simulator lends itself to easy modification.

The 5-kHz clock is intended as system clock during offset adjustment of the integrators. The 200-kHz clock is used as system clock to simulate normal operation. The test system requires a clock for driving the 5-channel multiplexer and the digital-to-analog converter (DAC) hold register. The clock simulator output is for this purpose externally connected back into the test system.

IX. Multiplexer

Figure 10 shows the five-position 10-bit multiplexer and the bit-switches of the test channel. The multiplexer sequencer shown in Fig. 11 is a simple 3-bit binary counter equipped with a mode switch for changing its sequence from 0 through 4 to 1 through 4. During dynamic test of all channels with a known DC input signal one can then, in the 0 through 4 sequence, reference the operation of the four channels to the digital input from the test channel. During observation of channels 1 through 4 with a low-frequency dynamic input signal, a check can be made of the uniformity between the analog channels. Figure 12 shows the connection of the mode switch. In positions 1 through 4, it bypasses the sequencer and provides a 3-bit address for the multiplexer. In positions 5 and 6, the dynamic sequencer is connected to sequence between 0 and 4 and between 1 and 4 respectively.

X. Test-System Operation

With the mode switch in "CHANNEL 0" position, the bit-switches are connected through the multiplexer to the DAC which is then adjusted for zero and FS, i.e., $\pm$5-V output. Zero-volt output is checked on a 4-digit digital voltmeter (DVM) and on an oscilloscope with the amplifier in a high-gain position. On the oscilloscope one can then study the switching of the LSB.

The integrators and the sample-and-hold circuits are initially zeroed with inputs grounded using clock 2 (200-μs repetition rate) for the integrators and clock 1 (5-μs repetition rate) for the sample-and-hold.

With the system input grounded, the analog-to-digital converter (ADC) offset is zeroed for each channel, while reading the DVM and scope with reference to channel zero. In adjusting the DAC for FS, the bit-switches of the test channel are used. In adjusting the analog channels for FS, a DC voltage is connected to all channels, which results in an integrator output voltage of 5 V after 5 μs. The hold circuit output is observed on a high-gain oscilloscope and all integrating resistors are adjusted so that the FS hold voltage is the same for all channels. All ADCs are then zero- and gain-adjusted in the test system scanning

mode. For further details, see the adjustment procedure in Table 1.

To permit an oscilloscope to be used with high gain for FS observation during FS adjustment of a channel, an offset is made to the DAC output in the test system, resulting in an output voltage near zero. This connection is shown in Fig. 13. For further details, see Table 1.

XI. Operation Results

The analog input channels were used during June 1972 as part of the successful Venus Radar Interferometer Experiment equipment. The unit performed without failure, and recalibration of the equipment at the Goldstone Venus Site (DSS 13) proved to be easy using the built-in test system.

Reference

1. Rourke, K. H., and Ondrasik, U. J., "Improved Navigation Capability Utilizing Two-Station Tracking Techniques for a Low-Declination Distant Spacecraft," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. VII, pp. 51–60. Jet Propulsion Laboratory, Pasadena, Calif., February 15, 1972.

Table 1. Adjustment procedure for analog input channels

Step No.	Procedure
1.	Adjust power supplies +5, ±15 to +5.00 and ±15.00 using 5-digit DVM. Observe changes from no load to full load. Readjust for full load and observe long term changes.
2.	For the DAC test, set the MODE CONTROL switch to channel 0; Channel 0 refers to the manual bit switches. Set all switches to '1' and adjust DAC zero offset for reading 0.00 V on DVM and high-gain oscilloscope.
3.	Set bit switches to 1 000---00 and adjust DAC gain for −FS or −5.00 V reading on DVM.
4.	Double check and readjust the zero reading.
5.	Double check and readjust the +FS readings.
6.	Observe the 0 and +FS readings long term.
7.	Ground inputs to all channels. Use clock simulator output 2 (200 μs) as system clock input, and adjust zero offset of integrator (test output 1). Observe output on high-gain oscilloscope.
8.	Ground inputs to all channels. Use clock output 1 (5-μs clock), adjust sample and hold zero offset. The internal offset during the sample period is positive. Adjust the output to read zero during the hold period. Observe on high-gain oscilloscope.
9.	Input an arbitrary DC voltage close to saturation yet observable on high-gain oscilloscope to all channels. Adjust all integrating resistor potentiometers for identical readings (clock output 2).
10.	Center set all offset and gain potentiometers for all ADCs. Input alternately ground and a DC voltage resulting in FS output. Adjust alternately all offset and gain potentiometers for all channels to converge to all zero and identical FS. Observe on high-gain oscilloscope, scanning all channels including the reference channel. The reference channel must then be changed between zero and FS adjustment. For continued observation of high-gain oscilloscope at zero volts, the DAC output must be FS offset (with offset switch) during the FS readings.
11.	Zero and FS adjustment of ADCs should, if possible, be set at points where the LSBs switch at the same point.
12.	In the 0–4 scan mode with either zero or a DC voltage input to all channels, the value of a bit-change as read on the oscilloscope may easily be identified by reference to the bit switches of the test channel.
13.	The test system affords considerable versatility, and a great many tests other than those listed above can no doubt be devised.

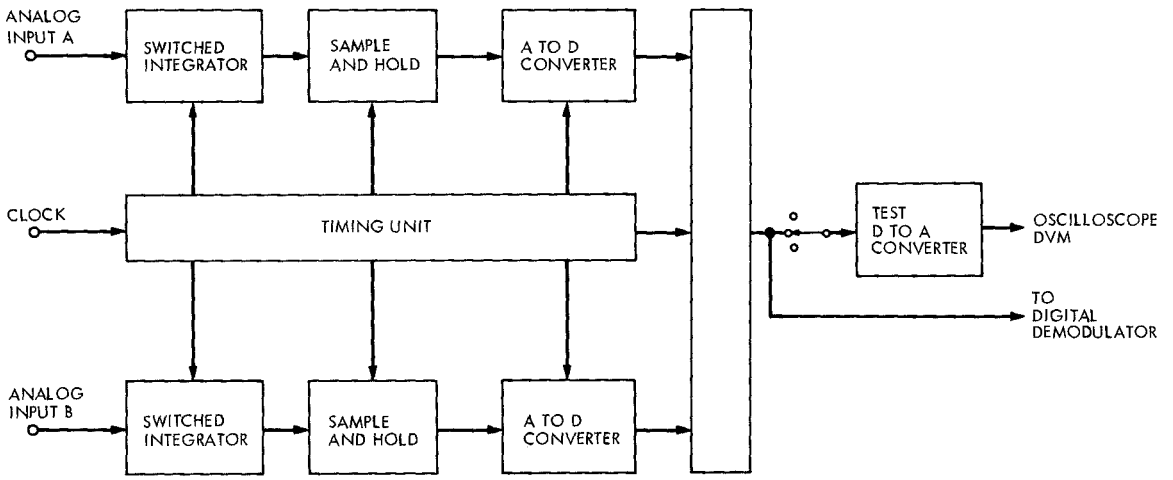

Fig. 1. Analog input integrate-and-sample system block diagram

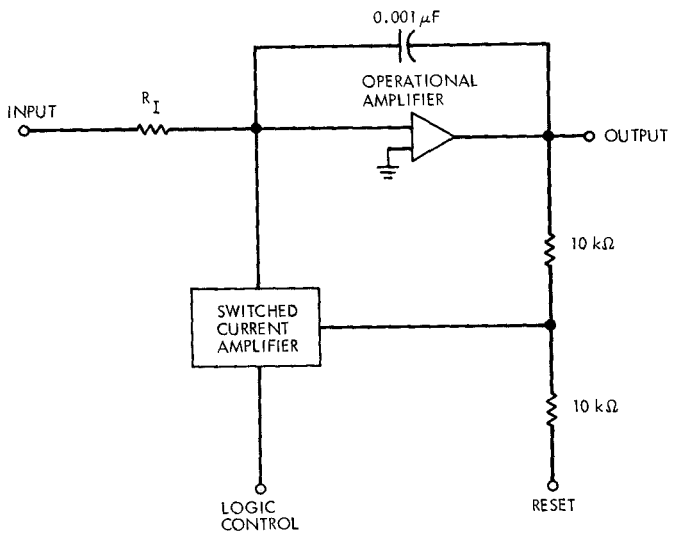

Fig. 2. Switched integrator block diagram

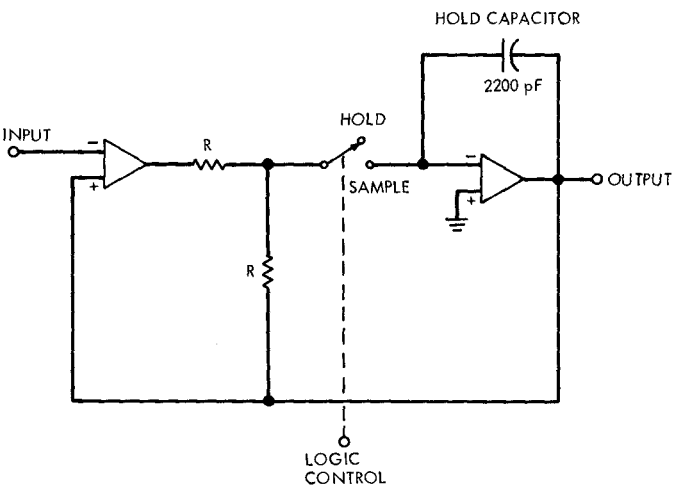

Fig. 3. Sample-and-hold amplifier block diagram

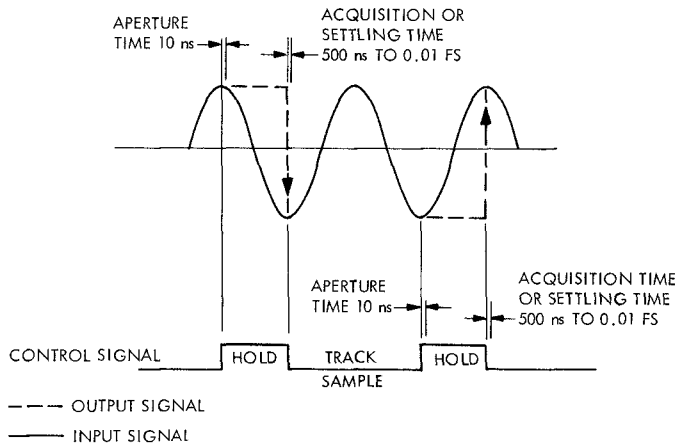

Fig. 4. Sample-and-hold timing chart and definitions

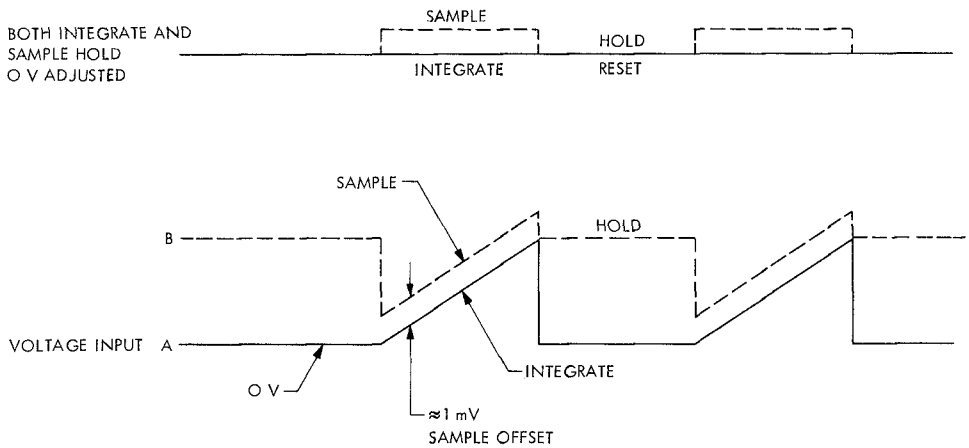

Fig. 5. Integrator output (A) and sample-and-hold output (B)

	S	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
+FS- LSB	0	1	1	1	1	1	1	1	1	1
+ 1/2 FS	0	1	0	0	0	0	0	0	0	0
+ LSB	0	0	0	0	0	0	0	0	0	0
ZERO REF	1	1	1	1	1	1	1	1	1	1
- LSB	1	1	1	1	1	1	1	1	1	0
- 1/2 FS	1	1	0	0	0	0	0	0	0	0
- FS	1	0	0	0	0	0	0	0	0	0

Fig. 6. 2's complement code definition

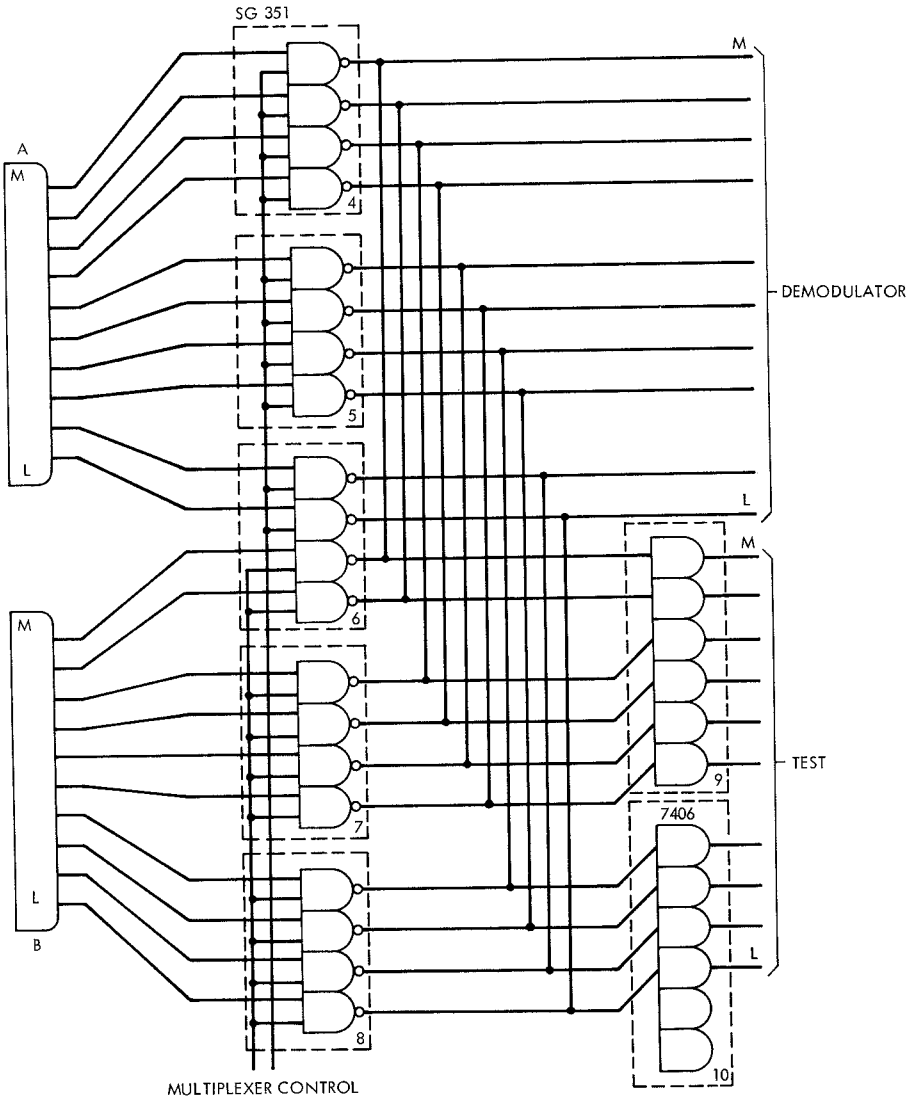

Fig. 7. Output digital demultiplexer

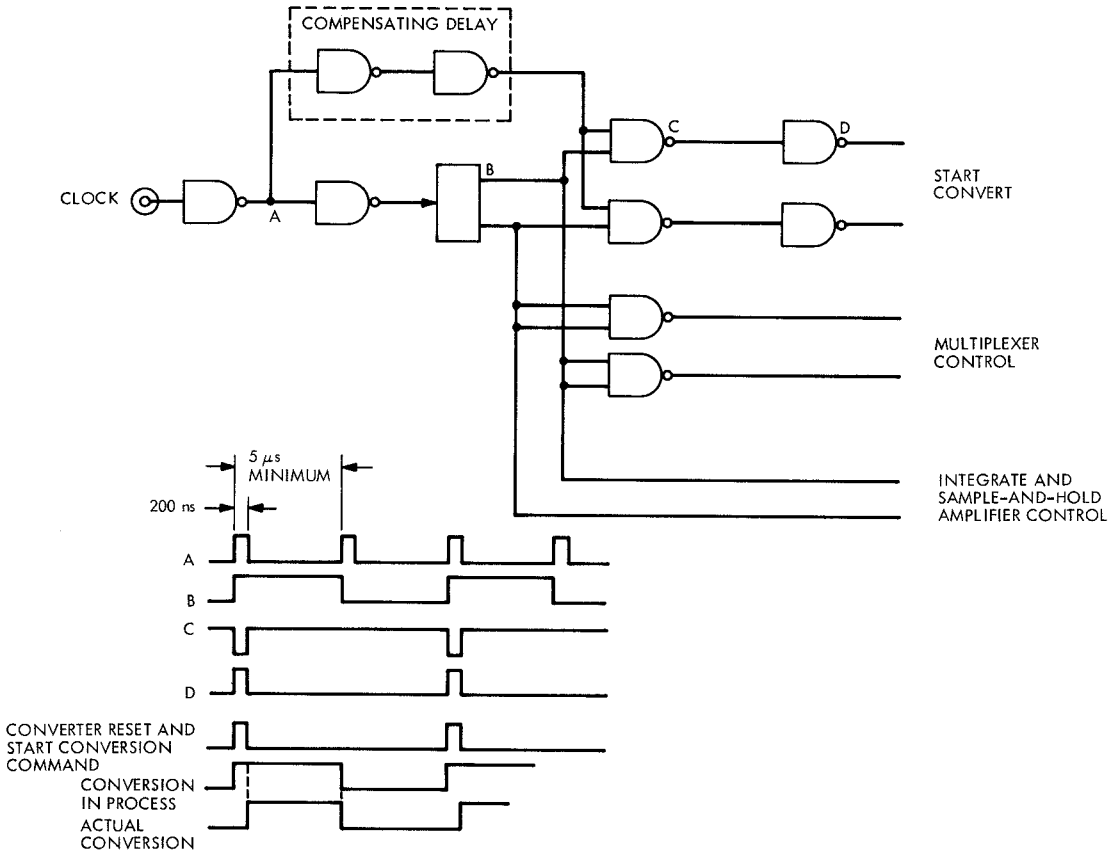

Fig. 8. Time control circuit

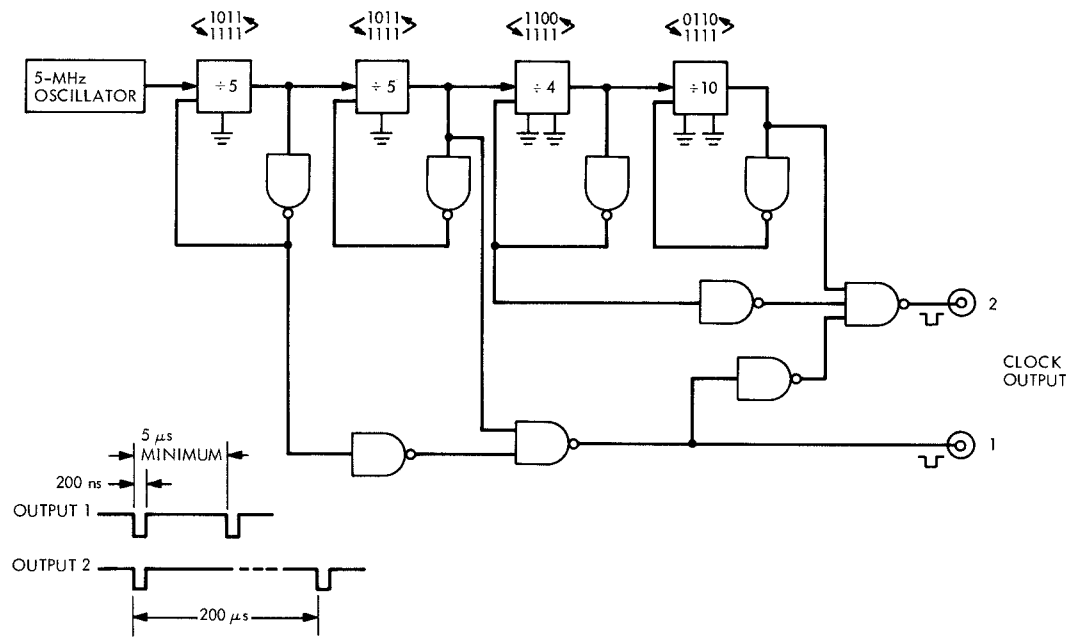

Fig. 9. Clock simulator

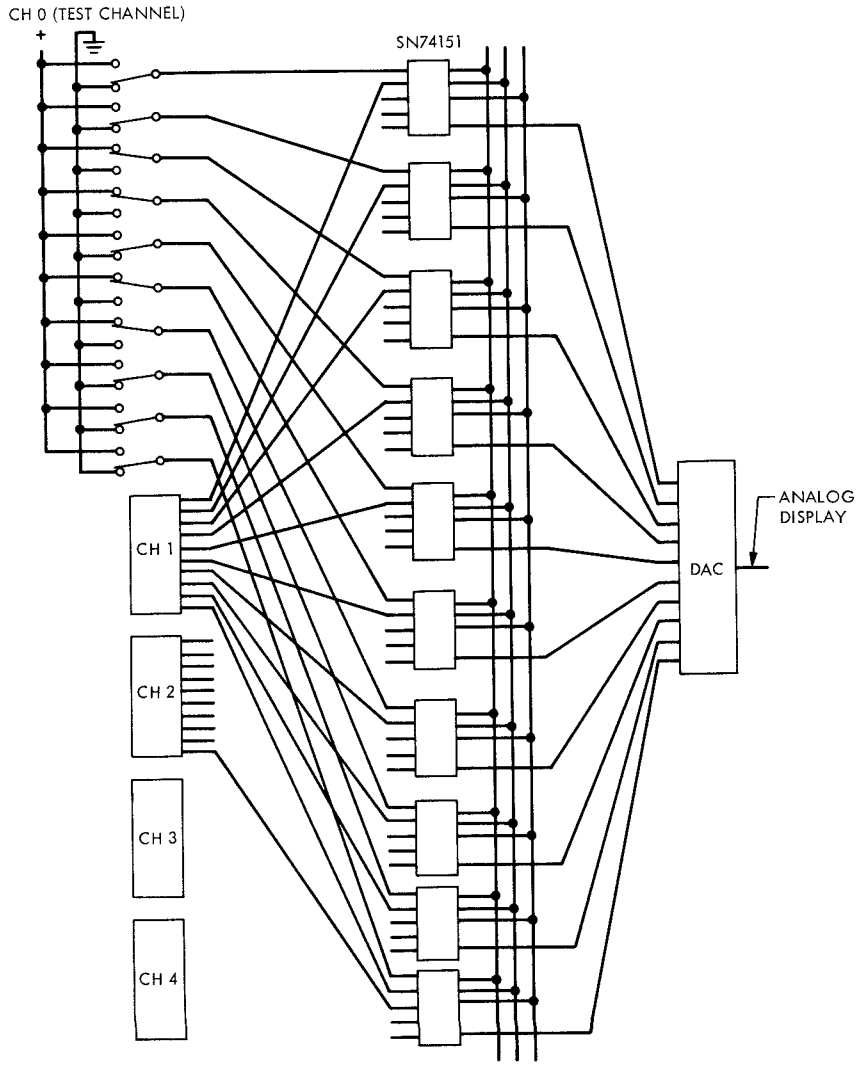

Fig. 10. 5-Channel multiplexer and test channel (bit switches)

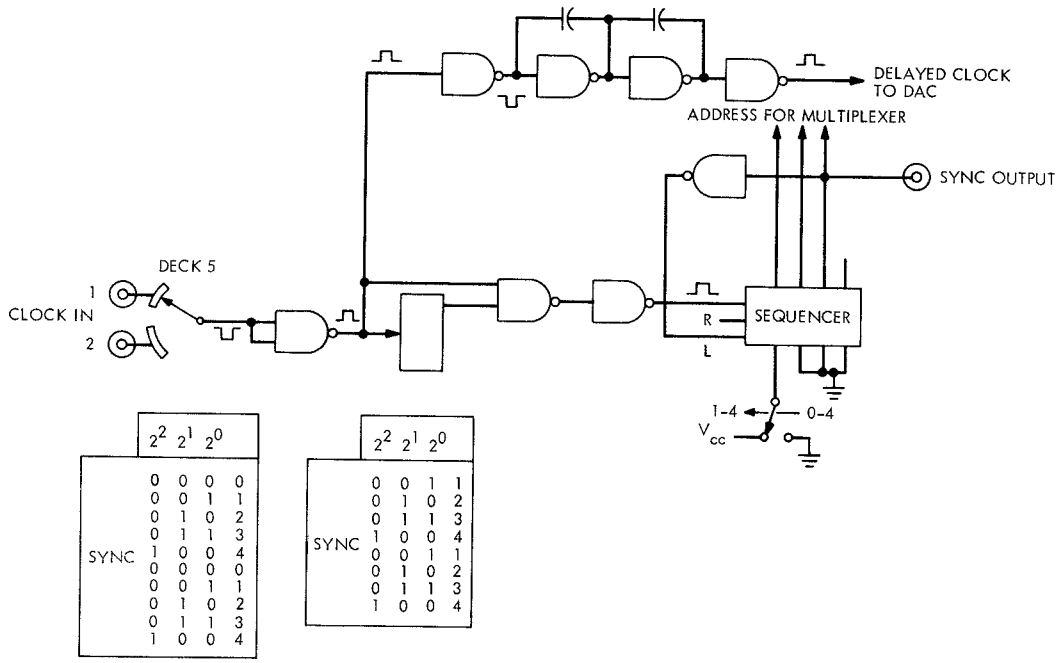

Fig. 11. Multiplexer sequencer

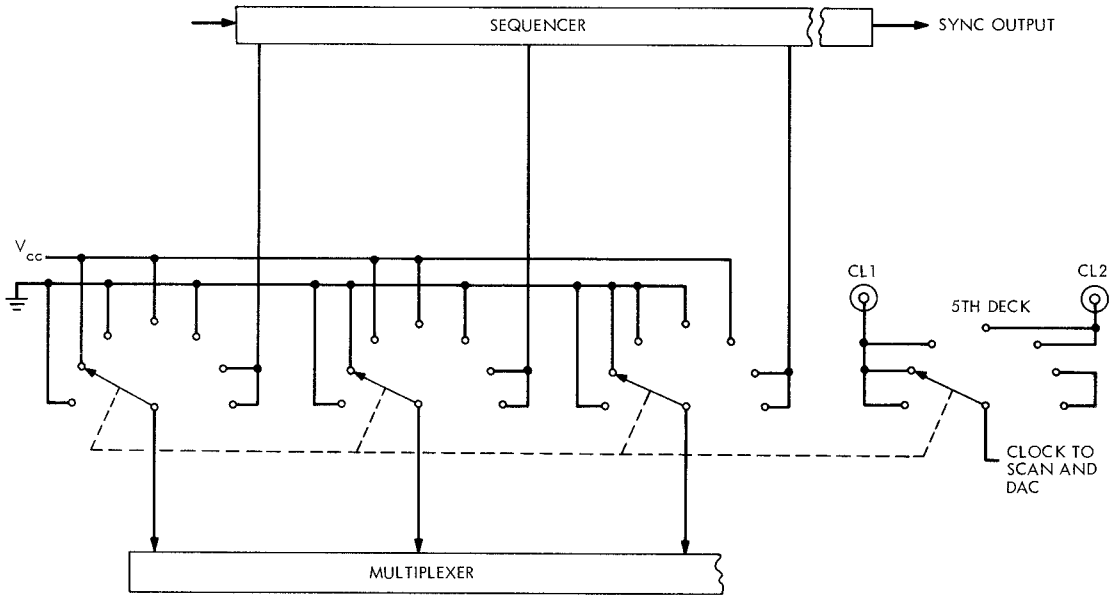

Fig. 12. Mode selector

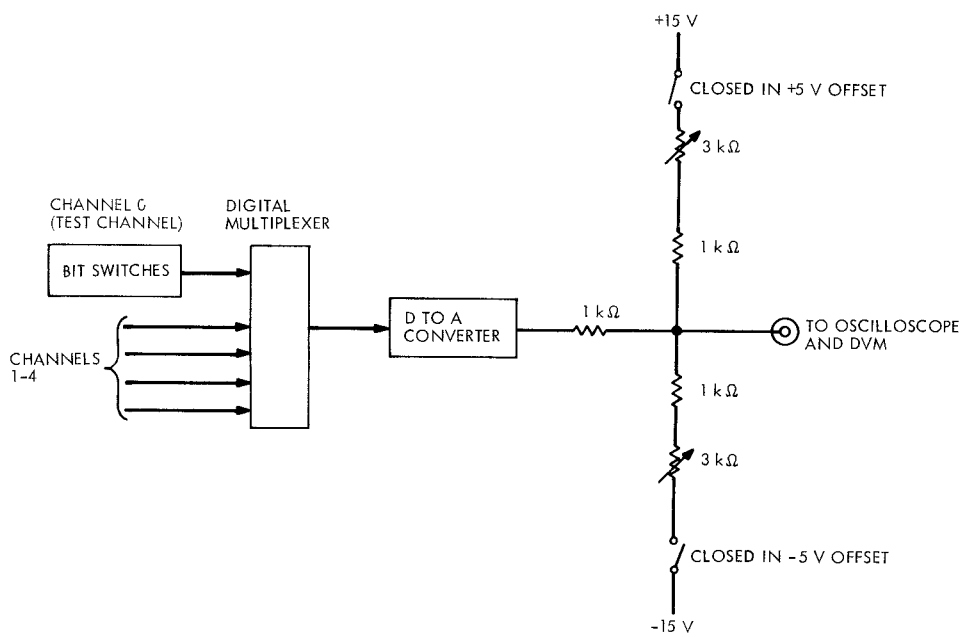

Fig. 13. DAC output offset circuit