A Scaled-Time Telemetry Test Capability for Sequential Decoding

S. Butman, J. Layland, and J. MacConnell
Communications Systems Research Section

R. Chernoff and N. Ham
R. F. Systems Development Section

J. Wilcher
DSIF Digital Systems Development Section

This article describes the motivation for, and development and initial testing of, a scaled-time telemetry test capability. The immediate need for this capability is to establish the sequential decoding performance of the data decoder assembly (DDA) for Helios and Pioneer, and the tests have been aimed at evaluating the suitability of the scaled phase-locked loop (PLL) for this task. The relevant parameters of limiter suppression, phase jitter variance, and phase jitter auto-correlation have been measured, and no discrepancy was found between the ×16-scaled PLL and the 12-Hz loop of the DSN receiver. Comparative sequential decoding tests have also been performed for 128-bit/s data; no discrepancy was found between scaled and unscaled performance at any modulation index, either near-optimum or high (70 deg), where the carrier reference noise is dominant.

I. Introduction

The purpose of this article is to describe the experimental setup and preliminary results of a time-scaled simulation of a convolutionally coded, sequentially decoded, coherent telemetry link. The need for such an approach arose when it became necessary to provide the Helios project as well as future Pioneer projects with an accurate estimate of link performance and design trade-offs at medium data rates. Medium rates are by definition data rates of the same order of magnitude as the bandwidth of the phase error process in the coherent reference signal, or more generally, data rates at which decoder memory is comparable to the memory of the phase-locked loop.

Such conditions arise at low received signal levels at end and post-end of missions and at stronger signal levels when transmission is contaminated by a turbulent medium like the solar corona, a planetary atmosphere, or during rapid descent of a probe.

Experimental performance estimation through simulation is necessary under the above conditions because accurate theoretical models of decoder behavior when the phase is not constant are not yet in existence (Ref. 1). The current state of decoding theory can accurately predict decoder performance only when the phase is constant over many constraint lengths. Finally, scaling up of the simulations to a higher speed than under normal operating conditions is necessary in order to accumulate the required amount of statistical data in a reasonable length of time. For example, to establish with reasonable confidence a bit error probability of 10^{-5} requires about 10^{8} bits. To gather this amount of data at 100 bits/s would take over 10 days. Similarly, establishing a block erasure probability (decoder overflow) of 10^{-3} for blocks of 1000 bits, would take 10 days.

II. Scaling the Tests

The block diagram in Fig. 1 depicts the system elements which require modification to provide a high-speed version of actual behavior at normal operating conditions. It is assumed that the front end noise is wideband, with a one-sided spectral density N_0. Primed variables denote scaled versions of the normal unscaled quantities, and x denotes the scale factor. There are several ways to achieve the required scaling of the system dynamics. The method we selected may be described as follows:

$N'_0 = N_0$	Wideband noise level unchanged
$P'_T = xP_T$	Total signal power scaled up
$R' = xR$	Bit rate scaled up
$\omega'_L = x\omega_L$	Loop bandwidth scaled up
$r' = r$	Damping ratio unchanged to preserve relative dynamics
$\alpha' = \alpha$	Limiter suppression factor unchanged to preserve relative dynamics
$\omega'_H = x\omega_H$	Prefilter bandwidth increase required to maintain the same input signal-to-noise ratio (SNR) to the limiter for $\alpha' = \alpha$
$\rho'_L = \rho_L$	Loop SNR unchanged
$E'_b/N'_0 = E_b/N_0$	Bit SNR unchanged
$m' = m$	Modulation index unchanged
$\tau'_i = \tau_i/x$	Loop filter time constants reduced
$K' = xK$	Loop gain increased

The above quantities obey the following relationships, which are documented by Tausworthe (Ref. 2)

$$E_b/N_0 = m^2P/N_0R$$

$$\rho_L = \alpha/\omega_L N_0$$

$$r = \alpha K\tau_2^2/\tau_1$$

$$\omega_L = (1 + r)/\tau_2(1 + \tau_2/r\tau_1)$$

and

$$\alpha = \alpha(\rho_H)$$

where

$$\rho_H = (1 - m^2)P_T/N_0\omega_H$$

$m = \sin\theta$, where θ is the modulation angle

Inserting the scaled parameters into the above formulas will verify that all the scale changes are achieved and the relative dynamics preserved where necessary.

Time-scaling of the subcarrier demodulator and symbol synchronizer assemblies (SDA and SSA) is accomplished through switch-selectable operating modes which match the actual (i.e., upscaled) data rates. Moreover, the losses in these assemblies are small and relatively insensitive to rate changes.

III. Test Techniques

The approach followed in evaluating the scaled-time telemetry test capability must minimize the test time required to build confidence in the correctness of the scaled parameters. The first tests therefore measured the global static PLL parameters, limiter suppression α, and phase jitter variance σ_ϕ^2, at specific signal strengths and compared these measurements with published results for the 12-Hz DSN PLL. Dynamics of the PLL behavior also influence strongly the performance of medium-rate telemetry, necessitating their measurement, in the form of the phase jitter autocorrelation function. In this case, both the 12-Hz DSN PLL and the scaled PLL had to be measured, as the desired parameters were not generally documented.

The ultimate criterion for acceptance of the results of the scaled telemetry tests is, of course, the equivalence of measured telemetry performance in both normal and scaled-time modes. This is most economically used at the mid-range data rates only (e.g., 128 bits/s), where reasonable duration tests can define the system performance. The anticipated plan is to test at 128 bits/s over a set of modulation indices near optimum, and to spot-check many data rates at one very high modulation index. For each data rate checked in this fashion, the modulation index will be set sufficiently high for the noisy carrier reference to be the dominant source of noise, and so that performance is poor enough to be measured in reasonable time without scaling. The total received power level will be set high enough so that the desired 10^{-4} deletion probability could be achieved with a lower modulation index. A successful match of performance at the high mod-index will, of course, indicate that the noisy reference losses are correctly scaled. Since we belive that the additive receiver noises will scale correctly, successful high mod-index comparison should also indicate overall success of the scaled test setup. Some prior test data (Ref. 3) exist for normal-time tests of performance near the optimum mod-index which can be compared against the scaled tests to identify any unexpected errors in the scaling assumptions.

No plans exist presently to test the scaled-time test configuration for uncoded telemetry. Since performance of sequential decoding is very critically dependent upon the adjacent-symbol correlation of the carrier reference noise, correct scaled-time performance of sequential decoding almost certainly implies that scaled-time tests of uncoded telemetry will also be correct. Future users of the scaled-time test capability for uncoded data will, of course, have the option of accepting this hypothesis or performing whatever additional tests they might need to validate the scaled-time performance for uncoded telemetry.

IV. The Scaled Loop Hardware Design and Initial Testing

The preceding sections have shown that, by scaling the receiver 12-Hz loop bandwidth, statistical data on bit error rates can be obtained in a time inversely proportional to the scaling number N used on the receiver. It was decided to scale the receiver loop bandwidth by 16, a factor which allowed a reasonable improvement in the speed of data acquisition without causing the data rates for the faster bit rates to exceed the capabilities of the telemetry decoding equipment.

For the scaling number under consideration (16), it was necessary only to scale the tracking filter and the predetection filter. (If extremely high scaling numbers are used, it may be necessary to increase the bandwidth of the IF amplifiers). Since B_L is being scaled, it can be shown that it is necessary to decrease τ_1 by $(N)^2$ and τ_2 by N, where $\tau_1 = R_2C$ and $\tau_2 = (R_1 + R_2)C$ in Fig. 2. For the case being evaluated ($N = 16$), τ_1 becomes 9.887 s and τ_2 becomes 8.5×10^{-3} s. The hardware implementation of the tracking filter consisted of modifying the values of R_1, R_2, and C in a standard DSN tracking filter module to provide the new time constants. The only other hardware modification required was the predetection filter amplifier. The bandwidth (BW) of this amplifier must be scaled (increased) by the scaling number N. For this test, the bandwidth was increased from the normal 12-Hz loop value of 2 kHz to the new value of 32 kHz noise BW. The hardware implementation consists of a four-stage, synchronously tuned amplifier. (The gain of this filter amplifier must be the same as that of the normal amplifier in order not to disturb the automatic gain control (AGC) performance of the receiver). For future experiments, the predetection filter could be a commercial crystal filter. This would enable tighter control of the bandwidth between units, as well as better bandwidth stability vs. temperature. The changed modules are identified in Fig. 3.

In order to verify that the receiver bandwidth had been properly scaled, several experiments were run. Input carrier power was set for all tests by the Y-Factor Technique (Ref. 4). First, the limiter suppression (α) characteristic was checked by measuring carrier power at the limiter output vs. loop threshold margin. This measurement was performed by a coherent amplitude detector and vacuum tube volt meter (VTVM). The results of the test can be seen in Fig. 4. Ideally, the scaled and unscaled α curves should be identical. If the α characteristic levels off at a lower margin in the scaled case, it would probably indicate an IF amplifier or limiter of insufficient bandwidth, or an insufficient noise bandwidth in the predetection filter amplifier. (If high-scaling numbers are used, it may be necessary to increase the BW of the IF amplifiers. This will prevent their influencing the predetection bandwidth, which should ideally be determined solely by the predetection filter amplifier). Since the curves for the scaled and unscaled cases are nearly identical, it appears that the predetection filter is indeed the determined BW, as desired.

The second test consisted of measuring the phase jitter (σ_ϕ^2) of the receiver voltage-controlled oscillator (VCO) as a function of margin. These data were obtained by employing the test translator as a signal source, and the UHF doppler detector as a dual phase detector, which allowed measuring the variance of the phase noise present on the VCO. The test configuration for this measurement is shown in Fig. 3. The UHF doppler signal (zero doppler + phase jitter) is phase detected against the station frequency standard. The phase shifter is required to set the reference phase in quadrature (to enable phase detection), with either of the two signals being phase detected in the dual phase detector. (The other signal is being amplitude detected.) For each data point (value of margin), both channels are sampled and recorded by the digital instrumentation system (DIS). The need for sampling both channels arises when a cycle slip occurs. For each cycle slipped at S-band, there appears a 90-deg shift in the phase at the UHF doppler detector. (This is due to a $\times 4$ multiplication between the point at which the UHF doppler is extracted and the S-band local oscillator output.) Therefore, if a cycle is slipped, the channel that was phase detecting is now amplitude detecting and vice versa. To prevent loss of phase data following cycle slip, both channels are recorded. When the tapes are processed, only the channel that is phase detecting is used. From those data, the variance (σ_{θ}^{2}) is calculated. As can be seen in Fig. 5, the data follow very closely those obtained with the normal 12-Hz loop. This further indicates that the receiver seems to be properly scaled.

The third test consisted of taking the autocorrelation of the phase jitter data. Each autocorrelation plot shows the time response of the loop at a particular margin. By plotting τ from each of these plots vs. margin, a plot is obtained that illustrates loop response vs. margin. Figure 6 is such a plot for both the scaled and unscaled loops. If the loop is properly scaled, the scaled loop will have a value of τ equal to $1/N$ of the unscaled loop at each margin. For convenience, the time (τ) scales of the two data sets shown in Fig. 5 are scaled by the scaling factor N. Therefore, the two curves will coincide if the loop is properly scaled. As can be seen, there is very close agreement between these two curves.

The results of this group of three tests seem to indicate that the receiver loop bandwidth was indeed scaled the desired amount over the range of loop margins considered.

V. Telemetry Tests

Testing of the scaled-time telemetry test capability using sequential decoding requires that several decoding test runs be performed using both the 192-Hz loop and the 12-Hz DSN receiver at identical (scaled equivalent) test conditions. To be convincing, these test runs must cover the range of data rates, SNRs, and modulation indices for which scaled tests are expected to be used. The scaling can be used at data rates of 256 symbols per second (SPS) (scaled to 4096 SPS) and lower. At scaled 512 SPS (8192 SPS) and above, the data decoder assembly (DDA) cannot operate successfully.

The test configuration for sequential decoding testing with scaling is shown in Fig. 7. It is identical to the configurations used for normal DSN testing of sequential decoding for Pioneer or Helios, except that the receiver modules for the 192-Hz loop are substituted for those of the 12-Hz DSN receiver PLL. The output from the test is a magnetic tape original data record (ODR) containing, for each data frame processed by the DDA, the number of decoding computations which were used in processing it. These ODR tapes are later analyzed off-line to determine the cumulative distribution of computations, which is then used to evaluate system performance. In the DSN station, the tests require the use of the simulation conversion assembly (SCA), the test transmitter, the antenna microwave assembly, the Y-factor assembly, a receiver and SDA, two telemetry/command processors (TCPs) with SSAs, and one DDA. The TCP–DDA–SSA string operates under control of nonstandard DSIF software—the DDA stand-alone-TCP verification program—and provides the ODR end-product of the tests. The second TCP–SSA string operates with the Mariner Mars 1971 (MM'71) Test Program No. DOI-5087-TP, and acts as a monitor for the telemetry channel, to verify station setup accuracy and identify drifts in parameters.

The SCA provides a pseudo-random data sequence for the test transmitter. The subcarrier frequency used is 32,993 Hz, and data rates of interest range from 16 to 4096 SPS. The biphase-modulated subcarrier in turn phase-modulates the carrier at the test transmitter, with a modulation index which may vary from 35 to 75 deg, depending upon data rate and other factors. This simulated telemetry signal is then processed by the station receiving equipment, much like the signal from a spacecraft. The "received" signal strength is set as required using the Y-factor measurement technique (Ref. 4) prior to the start of a test. The modulation indices are set by precision attenuators. Extreme care is required in this setup because of the sensitivity of decoding performance: the decoding erasure rate can vary by an order of magnitude with a 0.5-dB change in signal strength. After setup, the Test Program 5087 output monitors channel statistics, and when stable operation of the receiver and SDA is observed, the TCP/DDA program is activated to develop the ODR of decoder performance. The format of these ODR tapes is shown in Fig. 8.

Tests with the scaling test facility have been performed and the data analyzed for a real data rate of 256 SPS (scaled for 4096 SPS). The signal strength was set to that which would provide an ST_s/N_0 of 2.7 dB at 45-deg modulation index for both scaled and nonscaled tests. This value will produce an erasure rate of between 10^{-3}

and 10^{-4} at the optimum modulation index. Figure 9 shows the results of tests at several modulation indices. The computation distribution curve shown is a rather sensitive measure of channel behavior. The minor differences between comparable curves are well within the setup tolerance on the system, believed to be on the order of 0.4 dB. The high mod-index curves (70 deg) are interesting in that the carrier reference losses are the dominant noise source at this point. If the carrier reference losses failed to scale properly, we would expect it to be evident from these curves; since there is agreement, we conclude that the scaling of the 256-SPS data rate is successful. We expect this success to be repeated at lower data rates, but tests must yet be performed, lest some unexpected interference signal, or some other nonscaled or nonscalable artifact of the DSN receiver/SDA/SSA systems, contribute a larger than expected share to the telemetry system losses.

VI. Summary and Future Plans

This article has described the motivation for, and development and initial testing of, a scaled-time telemetry test capability. The immediate need for this capability is to establish the sequential decoding performance of the DDA for Helios and Pioneer, and the present tests have been aimed at evaluating the suitability of the scaled PLL for this task. The relevant parameters of limiter suppression, phase jitter variance, and phase jitter autocorrelation have been measured, and no discrepancy was found between the $\times 16$-scaled PLL and the 12-Hz loop of the DSN receiver. Comparative sequential decoding tests have also been performed for 128-bit/s data; no discrepancy was found between scaled and unscaled performance at any modulation index, either near-optimum or high (70 deg), where the carrier reference noise is dominant.

Further testing will be performed of the scaled-time telemetry test capability, and productive use made of it, at DSS 71, where long-duration tests are in progress to establish DDA performance. At each of the Helios data rates where scaling can be used, a very high modulation-index comparison test will be run to verify the scaling of noisy reference losses before the planned tests of several mod-indices and power levels are run.

References

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3. Lumb, D., Private Communication at Helios Working Group Splinter Session, Sept. 27, 1973.
4. *DSIF Program Library: Documentation for Y-Factor Computer Program*, DOI-5343-SP-B, 29 Sept. 1972 (JPL internal document).

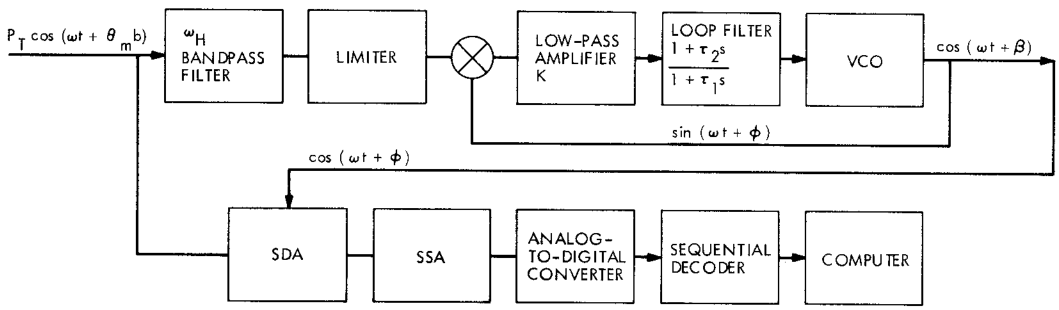

Fig. 1. Receiver block diagram

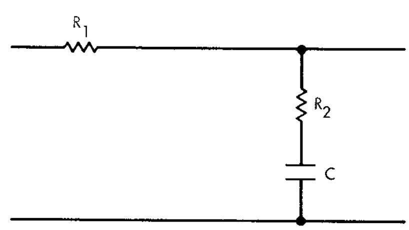

Fig. 2. Basic tracking filter

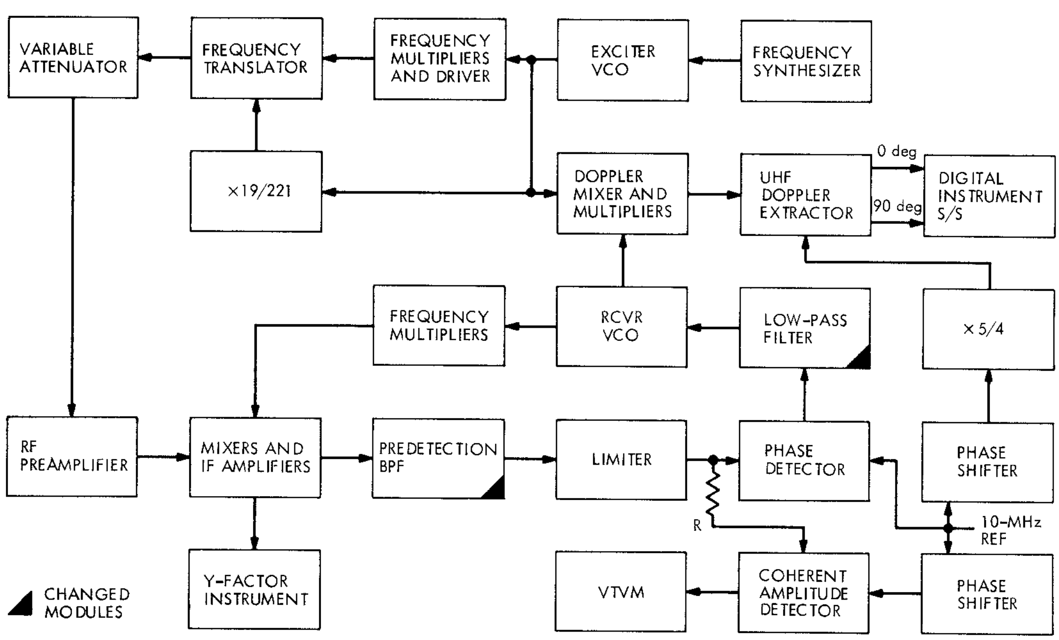

Fig. 3. Receiver/exciter doppler system

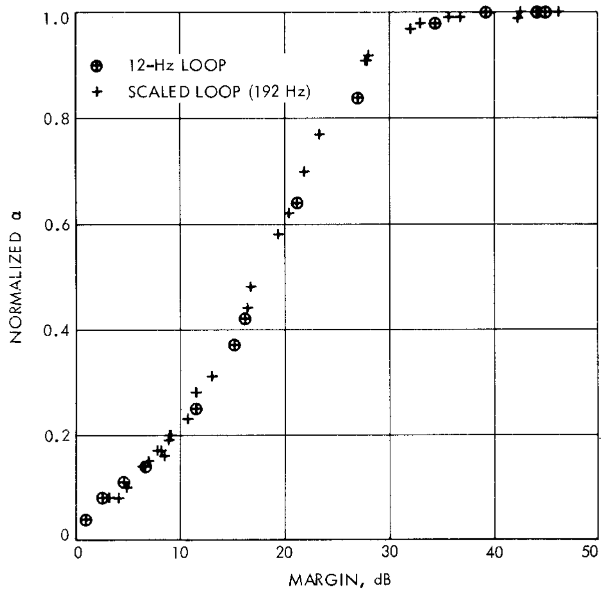

Fig. 4. Limiter suppression factor vs. loop threshold margin

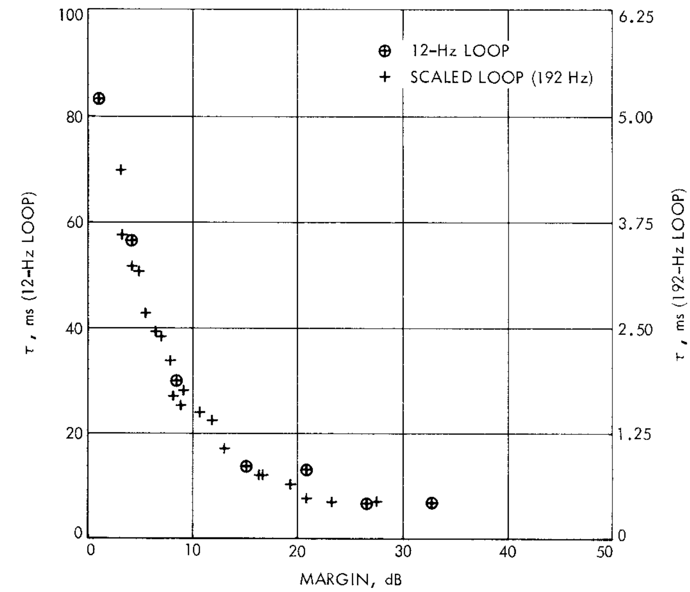

Fig. 6. Effective loop time constant vs. loop threshold margin

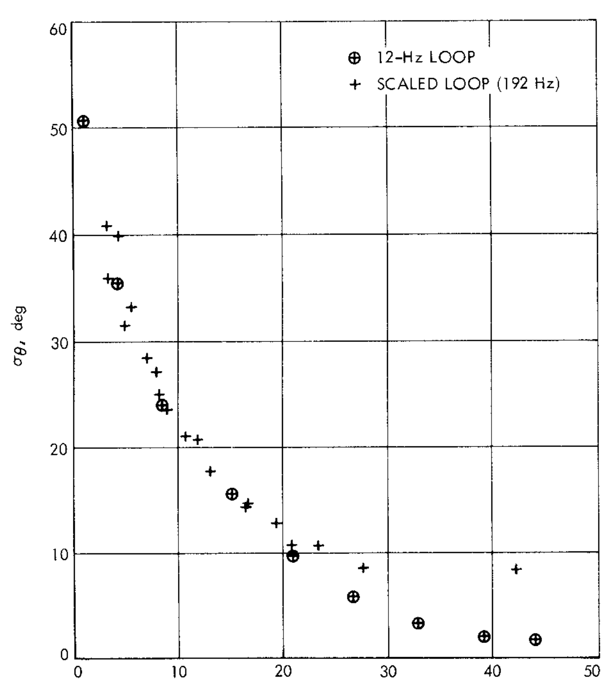

Fig. 5. Variance of loop jitter vs. loop threshold margin

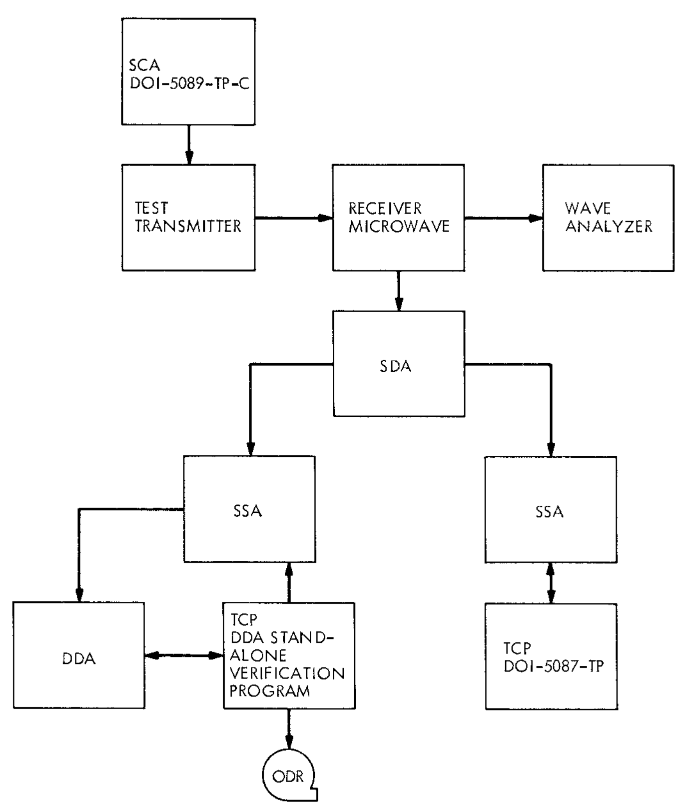

Fig. 7. Telemetry test configuration

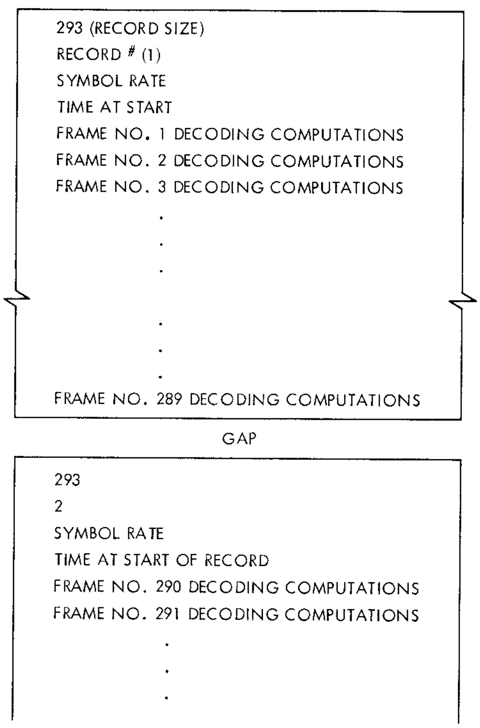

Fig. 8. ODR data tape format

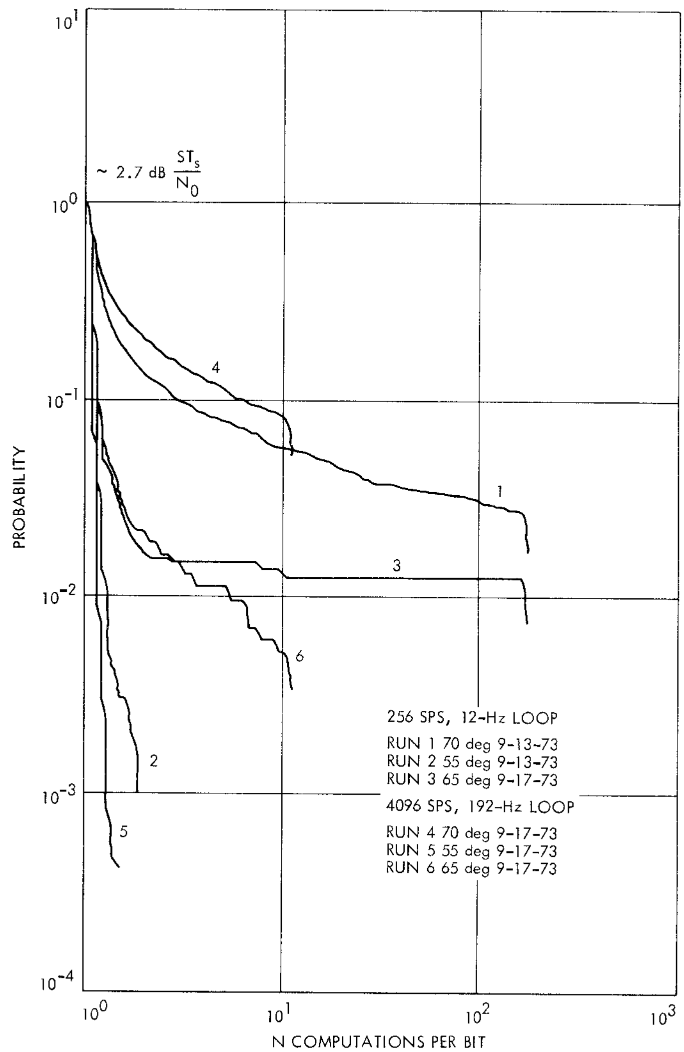

Fig. 9. Computation distribution curves, CTA-21 DDA test