Arithmetic Processing Unit

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The arithmetic processing unit described in this article is being developed to provide more meaningful numerical data from meters mounted in the antenna portion of high-power transmitters. This unit will compute directly changes in temperature, power dissipation, and water flow levels. The design constraints, requirements, and concepts are discussed.

I. Introduction

Because of the need to provide more meaningful numerical data from meters mounted in the antenna portion of the high-power transmitters, an arithmetic processing unit is being developed. These meters make up the indicator portion of various calorimeters located within the closed cooling system of each high-power transmitter. The analog output from these meters indicates the temperature and water flow rates within these closed cooling assemblies. The arithmetic processing unit uses these meter readings to calculate temperature variations and power dissipation within each assembly. The value of this information is that it provides a method of determining power dissipation within critical areas of the high-power klystron; these power dissipations, if excessive, could destroy the klystron.

Previous methods for calculating the dissipated power have required climbing the antenna, taking the needed meter readings, and then manually calculating the power dissipated from the equation

$$\mathrm{PW} = 0.264\,(\Delta T) \cdot \mathrm{FLOW}$$

where

PW = power dissipated by the closed assembly in kilowatts

ΔT = change in temperature in °C

FLOW = velocity of water in gallons per minute

Because of the time required and the frequency of the checks, little protection was provided from variations in power dissipated within the klystron. In a future modifica-

tion, as part of the transmitter automation, these data will be available for display in the control assembly; however, the calculations must still be performed manually. This method still allows only random monitoring of the klystron. The arithmetic processing unit is designed to provide continuous display of temperature change and power dissipation within the high-power klystron and, in this way, provide a more concise and convenient indication of each transmitter's performance.

II. Design Constraints

An analog signal corresponding to the meter readings is converted to a three-digit, binary-coded decimal (BCD) within the data collection unit (Ref. 1). It is then transmitted to the ground control area from the antenna over a single three-pair cable. The data are then entered into the multiplexing circuit of the arithmetic processing unit as illustrated in Fig. 1. The proper meter readings are selected and entered into the processing unit to calculate the parameters which are to be displayed. Thus, two major constraints were placed on the design of the arithmetic processing unit corresponding to the input and output requirements of the display unit and the data collection system, respectively:

(1) The input requirements are a multiplexed 12-bit (three-digit BCD), parallel-entered data stream with individually latching lines from the data acquisition unit.

(2) The output requires a multiplexed 12-bit (three-digit BCD), parallel data output with individually latched, three-digit parameters.

III. Design Requirements

The arithmetic processing unit is required to perform a programmed series of arithmetic operations on data received from the data collection system. These data may consist of up to 16 three-digit parameters for each series of calculations. These parameters are then used as operands in an equation such as

$$\mathrm{PW} = K(T_1 - T_2) \cdot \mathrm{FLOW}$$

or

$$\mathrm{PW} = K\left\{[(T_1 - T_2) + (T_3 - T_4)]\frac{F_1}{2} + [(T_5 - T_6) + (T_7 - T_8)]\frac{F_2}{2}\right\}$$

where

PW = power dissipated in klystron assembly in kilowatts

T_1, T_3, T_5, T_7 = temperature of water leaving klystron assembly in °C

T_2, T_4, T_6, T_8 = temperature of water entering klystron assembly in °C

F_1, F_2 = velocity of water in gallons per minute

The program for the equation used is contained in an eight-bit read-only memory, of which four bits are used as a machine language (*ones* and *zeros*) operation code and the remaining four are used as a memory address.

IV. Design Concepts

Based on the design constraints and equation complexity, the arithmetic processing unit was designed around an input/output multiplexer, a random access memory, a calculator chip, and a read-only memory. As shown in Fig. 2, the arithmetic processing unit consists of the units described below.

A. An Input/Output Multiplexer

The input/output multiplexer allows the unit to calculate many similar parameters and display them on the corresponding display panel. The circuit consists of gates which allow only one set of meter readings to be entered into the random-access memory during each calculation cycle. It also enables the correct display panel to accept the new parameter.

B. A 16- × 16-Bit Random-Access Memory

The random-access memory is used to store data during the calculations. This circuit accepts parallel inputs from the input multiplexer or the output register. The data in a memory location are sensed serially by the calculator circuit and are used as an operand in the equation.

C. A Calculator Circuit

The calculator circuit, built around a MOSTEC 5010P, four-function calculator chip, provides the necessary arithmetic functions. This circuit, which is controlled by the function generator, accepts the addressed data from the random-access memory, performs the selected arithmetic operation, and enters the result into the output register.

D. An Output Register

The output register holds the output data from the calculator while they are being entered into an addressed memory location or a display location.

E. A Read-Only Memory and Function Generator

The read-only memory and function generator control the sequence of all operations in the unit. The read-only memory consists of an eight-bit serial shift register which provides a four-bit memory or display address and a four-bit operation code to be used by the function generator. The function generator consists of 10 sets of sequenced operations; for example, one sequenced operation enters data into the calculator, while another loads data into the calculator and then subtracts the entered data from the data previously entered. These sequenced operations are selected by the four-bit operation code from the programmed read-only memory. The reason for this method of selecting the sequenced operations is that it requires only a modification of the programmed read-only memory to alter the function computed, as well as the memory address and display locations used.

V. Future Development

The arithmetic processing unit, as described, has been breadboarded. The unit is now being evaluated for its compatibility with the existing data collection system and its production considerations.

Reference

1. Smith, R. H., "Data Collection System for the Dual-Carrier Exciter," in *The Deep Space Network Progress Report for March and April 1973*, Technical Report 32-1526, Vol. XV (this issue). Jet Propulsion Laboratory, Pasadena, Calif., June 15, 1973.

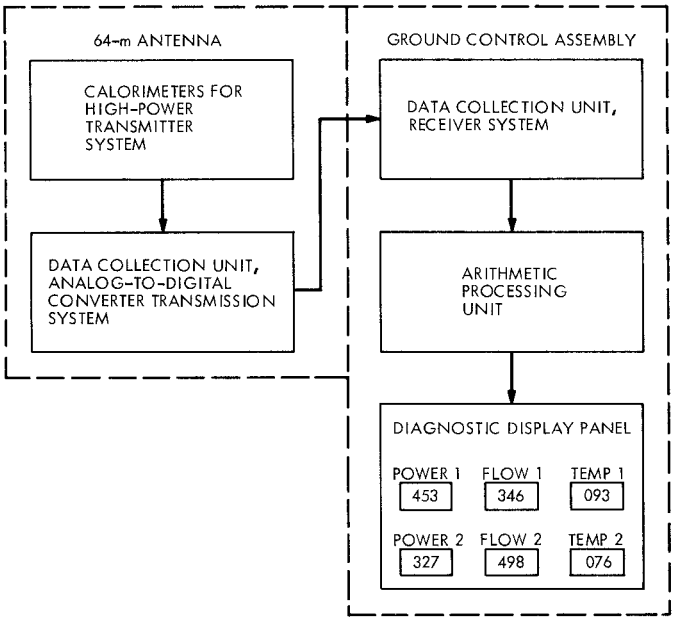

Fig. 1. Interfacing to arithmetic processing unit

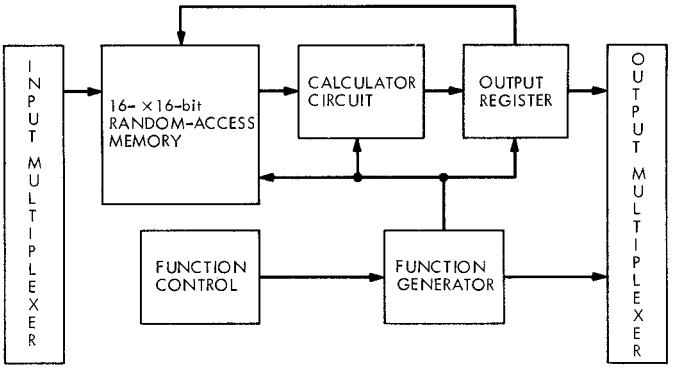

Fig. 2. Arithmetic processing unit block diagram