Bit Synchronizer for Sample Data Antenna Pointing System

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In the continuous effort to computerize antenna pointing and control systems at the DSN stations, sample data systems are required. As a result of modular subsystems being readily available commercially, the sample data systems are designed in accordance with a decentralized system design philosophy. A number of smaller subsystems are located physically close to the data sources. The subsystems feed data to collection centers which in turn feed data to the computer. The only connection between subsystems, collection centers, and computer is a single coaxial cable. Since there is no separate clock signal, bit synchronization must be extracted from the data signal in order to recover the serial binary data. This article describes a particularly simple bit synchronizer phase-locked loop especially designed for this noise-free environment. The performance of the loop has been analyzed and qualitatively verified on a laboratory breadboard model.

I. Introduction

In the continuous effort to computerize antenna pointing and control systems at the DSN tracking stations, sample data systems are required. As a result of such sample data systems being commercially available in cost-effective modular form, the sample data systems in question are designed according to the decentralized sample data system design philosophy. The analog-to-digital conversion is performed physically close to the data sources. Only a single coax cable is required to serially transmit the data from the subsystems to data collection centers and from there to the computer in the control room. At the receiving sites at the collection centers and at the computer site, one needs to recover the bit synchronization from the received data.

The bit synchronizer described in this article was designed for the purpose mentioned above. The loop is easy to implement. The mean acquisition time and phase jitter

have been analytically determined. The loop's performance has been qualitatively verified in a prototype breadboard model.

The bit synchronizer provides the bit sampling times for the received bit stream. Since the received signal is virtually noise-free the data can be recovered by sampling at the midpoints of each bit. The bit synchronizer, which is a first-order phase-locked loop, provides the bit midpoint sample timing. The received data are clocked into a serial input shift register for further processing.

For this application, where the received signal experiences no doppler shift, a first-order loop is sufficient to provide the required synchronization. The phase detector of the loop is based on sampling the point in time where the loop expects that the bit transition occurs (Refs. 1 and 2). For high signal-to-noise ratio systems it has been shown in Ref. 2 that one sample per transition is the optimum number of samples per transition to minimize the timing error jitter. More samples will not reduce the jitter except at low signal-to-noise ratios. Since the data are hard limited, the loop performance cannot be improved by quantizing the transition sample to more than one bit.

When considering random binary data, a transition detector is required to determine if a transition has occurred. This is employed in the present bit synchronizer. An error-normalizing circuit is also included. The function of the error-normalizing circuit is to make the sign of the error voltage dependent solely on the location of the transition and not on whether it is a positive to negative or negative to positive voltage transition (Refs. 3 and 4). The error signal is the sign of the sample taken at the expected transition time. The transition detector and the error normalizing circuit both operate on samples taken at the mid-bit time. The mid-bit time is also used to clock the serial binary data into a receiving serial input register.

II. Functional Description

For reference to the following discussion see the conceptual system block diagram and sample timing diagram in Fig. 1 and the detail control circuit for the voltage-controlled oscillator (VCO), Fig. 2.

The VCO provides a squarewave output of a frequency twice the bit rate. The true and complement output $a(t)$ and $\overline{a(t)}$ provide the data transition sample pulse and the mid-bit sample pulse respectively. When the phase-locked loop (PLL) is in lock, the leading edge of timing signal $a(t)$ occurs at the bit transition and the leading edge of timing signal $\overline{a(t)}$ occurs mid-bit.

The leading edge of timing signal $a(t)$ is used to sample the input data to determine the sign of the present phase error and to derive the error signal. The leading edge of timing signal $\overline{a(t)}$ is used to sample the input data to determine whether a transition occurred or not. If a transition occurred, a binary-valued error voltage is applied to the VCO. If a transition did not occur, a voltage that is midway between the two binary values is applied to the VCO. This provides an output frequency from the VCO, when there is no transition, that is equal to the received data rate.

Storage is required as follows: A bit is sampled at mid-bit time and stored. The sign of the error signal is determined half a bit time later. The error signal together with the output from the transition detector is stored at the following mid-bit time in order for the control voltage to be available to the VCO for a full bit time.

III. Sample and Storage

The following is a detailed functional description of the timing and storage operation shown in Fig. 1. Time t_1 is the point in time where the data is first sampled and then stored in storage element S1. At time t_3 the delayed data stored in S1 is added mod 2 to the present data and the sum is stored in S2. The output from S2 then indicates whether a data transition occurred at time t_2. At time t_2 the data is sampled and stored in S3. The output from S3 is added mod 2 to the output from S1, which serves as the normalizing term. This addition will assure the independence of the sign of the error signal from the direction of the transition. At t_3 the normalized sign of the error signal E is stored in S4. The output from S2, the transition detector, remains for one full bit time between t_3 and t_5. The output from S4, the sign of the error signal, remains for the same length of time.

IV. VCO Control

As shown in the conceptual system block diagram, Fig. 1, the outputs from S4 (the sign of the error signal) and S2 (the transition detector output) control the logic which applies a binary-valued control voltage to the VCO if a transition occurred. If a transition did not occur, a voltage halfway between the binary-valued correction voltages is applied to the VCO input.

The halfway voltage applied to the VCO in the no-transition case is adjusted so that the sample rate out of the timing circuit is equal to the incoming data rate.

VI. VCO Control Circuit

If one inspects the two-variable truth table for T and E shown in Fig. 2 together with the adjacent desired control voltage table, one can deduce that simple resistive network summing voltages corresponding to two other variables F_1 and F_2 will produce the desired VCO voltage.

Variables F_1 and F_2 can be expressed by

$$F_1 = \overline{T} \oplus E$$
$$F_2 = E. \tag{1}$$

Whenever a transition occurs, i.e., $T = 1$, both F_1 and F_2 take on the value of E, so that the maximum output voltage occurs at the resistor network summing junction when $E = 1$ and the minimum occurs when $E = 0$. When no transition occurs, i.e., $T = 0$, then either $F_1 = 1$ and $F_2 = 0$ or $F_1 = 0$ and $F_2 = 1$; in either case the voltage at the summing junction is the average of the minimum and maximum values. The center frequency adjust potentiometer is used to force this average voltage to correspond to the VCO center frequency.

Potentiometer R_2 in Fig. 3 provides a control of the amount of phase correction during one bit time; i.e., it acts as a bandwidth adjustment.

VII. Performance

Since this system receives a signal via a closed circuit, the effect of thermal noise can be neglected. However, the timing error jitter, defined by

$$\sigma_T^2 = \lim_{N \to \infty} \frac{1}{N} \sum_{i=1}^{N} (e_i)^2 \tag{2}$$

where e_i is the timing error expressed in seconds at time t_i, will not be zero. In fact the timing error will be determined by the amount of the timing adjustment (or phase change) during one bit time. Denote ΔT as the timing adjustment, expressed in seconds, that occurs in one bit time, or T_b seconds. Then the minimum timing jitter after acquisition will be given by

$$\sigma_T^2 = \frac{(\Delta T)^2}{4}\left(1 - \frac{2P}{3}\right) \tag{3}$$

where P is the bit transition probability. Hence the smaller the relative timing adjustment, the smaller the timing jitter. If, as would be expected in practice, the transition is not equidistant from successive samples, then the timing jitter is increased to as much as

$$\frac{(\Delta T)^2}{2}\left(1 - \frac{P}{3}\right).$$

Since the data is obtained from the data stream by sampling the data bit at the midpoint of the bit, jitter is not very important as long as it is small compared to $T_b/4$ seconds. However, ΔT does affect the acquisition time T_a and the tracking range. Following the methods in Ref. 2 it can be shown that for the first-order loop with no frequency offset but worst-case initial timing error, the mean acquisition time T_a is given by

$$T_a = \frac{T_b}{P}\left(\frac{T_b}{2\Delta T} - 1\right). \tag{4}$$

To determine the frequency tracking range, we observe that the average bit period can be increased or decreased by $P\Delta T$; thus the frequency can be changed by approximately

$$\frac{P\Delta T}{T_b^2}$$

and the fractional tracking range R is

$$R = \pm \frac{P\Delta T}{T_b}$$

A second-order phase-locked loop should be used when this tracking range is inadequate. This generally occurs when large frequency offsets may occur due to oscillator instability. The tracking range is then determined by the range of voltages which can be applied to an integrating capacitor. The above relationships for jitter and acquisition time are approximately valid for the second-order case if the loop is overdamped and the frequency offset is small.

An experimental loop has been constructed with $\Delta T/T_b \approx 0.05$. With a transition probability of 0.5, the rms timing jitter was 2% and the tracking range was $\pm 2.5\%$. The loop was then modified to an overdamped second-order loop which achieved a tracking range of $\pm 7.5\%$.

References

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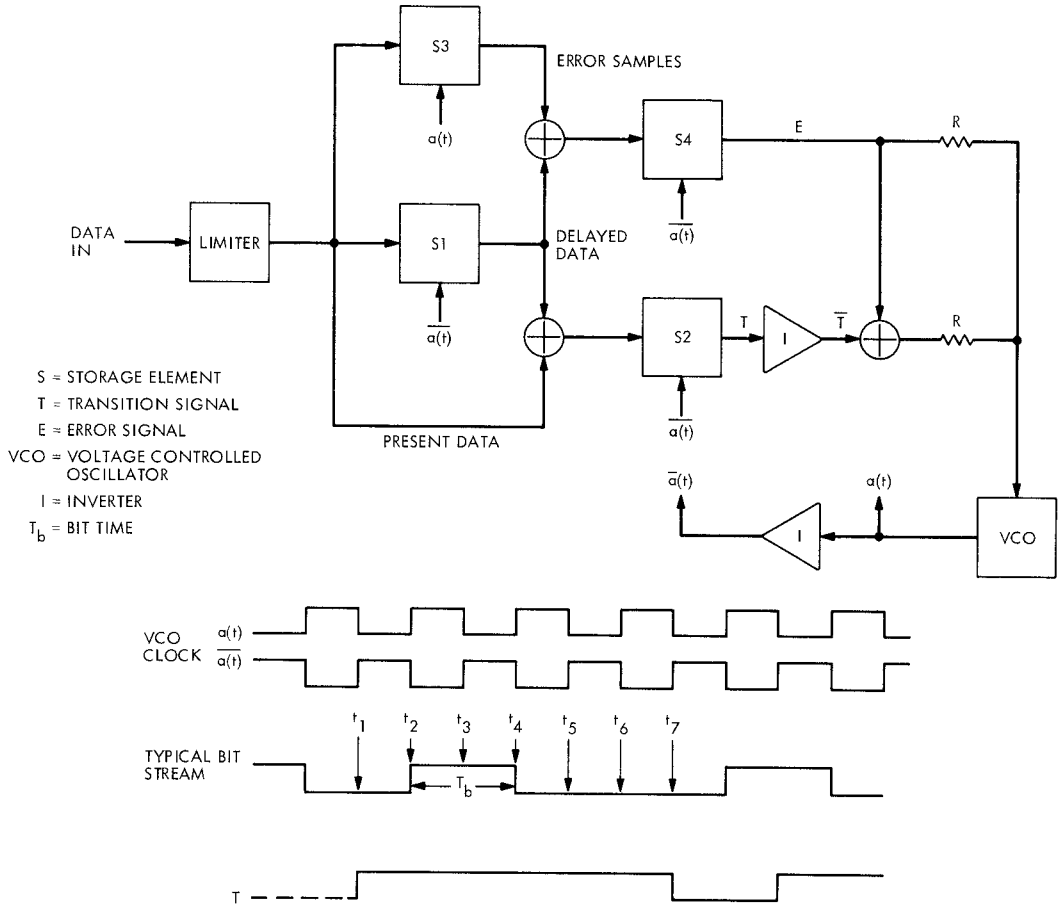

Fig. 1. Conceptual system block diagram and sample timing diagram

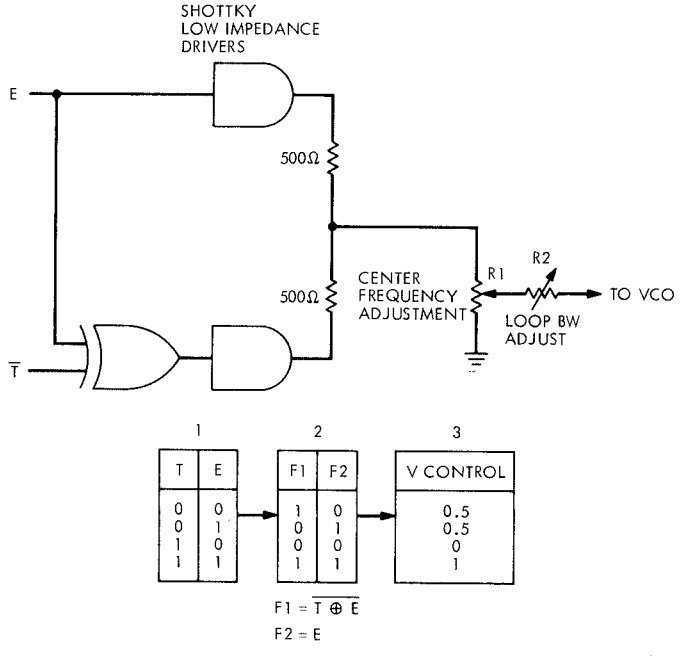

Fig. 2. Detail of VCO control logic