Block IV Subcarrier Demodulator Assembly Design

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A design effort was undertaken during the past two years to design and build a Block IV Subcarrier Demodulator Assembly. The salient features that were to be incorporated were: (1) capability of manual or computer control, (2) small size, (3) higher data rate capacity (500,000 symbols/s), and (4) improved subcarrier tracking in the presence of high doppler rates. This report reviews the design and indicates the current status of the development project.

I. Introduction

The Block IV Subcarrier Demodulator Assembly (SDA) is a new assembly scheduled for incorporation into the DSN in FY 1975. The Block IV SDA is a second-generation development that has evolved from the basic development work done on the Block III SDA started in 1968. To appreciate the new design, a functional comparison between the Block III and Block IV SDA is listed in Tables 1 and 2 to illustrate the difference in the designs. Comments have been made where significant differences occur.

II. Block Diagram of Block IV SDA

It will be noted from the block diagram (Fig. 1) that the RF modules are designed for remote control (i.e., both the voltage variable attenuators and phase shifters are controlled from the control unit assembly) to allow either manual or computer control of the SDA.

This block diagram differs from the Block III SDA in that the error channel uses part of the quad intermediate-frequency (IF) channel. This reduces the required hardware and has the effect of improving the loop performance since the data and data estimate paths have more nearly equal time delays. A further improvement in path delay matching will be realized since increasing the package density has resulted in more of the signal path contained in each module and fewer system cables. Matching the time delay path (data and data estimate) is important since it directly affects the loop gain and therefore tracking performance.

III. Signal and Noise Level Profile for the Block IV SDA

The criteria utilized in this proposed design were as follows:

(1) Gain switching using combinations of 0-, 7-, 13-, and 20-dB attenuators is required before and after the phase switch in the quadrature generator to maintain maximum signal (and noise) level (consistent with linearity) vs subcarrier leakage at the phase switch. Gain switching is required due to the quadrature generator subcarrier leakage problem (i.e.,

the signals at the input to the quadrature generator are carrier times subcarrier times data, *and* subcarrier estimate. The output spectrum is not simply the product of the input, but is the product plus an unwanted additional component of the subcarrier estimate). A comparison was made between the Block III and Block IV performance for this problem and an improvement of 10 dB was achieved. This improvement was achieved by using devices with greater linear dynamic range.

(2) Bandwidth switching, after the quadrature generator, was implemented using six discrete bandwidths. Bandwidth selection was made using the criteria that

$$\frac{ST_{sy}}{N_o} = -1\,\text{dB}\ (\text{for}\ 5 \leq R_{sy} \leq 500\,\text{sps})$$

$$\frac{ST_{sy}}{N_o} = -4\,\text{dB}\ (\text{for}\ 500 \leq R_{sy} \leq 500\,\text{ksps})$$

determine the lower symbol rate allowed to guarantee system linearity. A 7-dB crest factor was allowed between the rms noise level and the 1-dB gain compression level for each system component.

Each bandwidth was chosen for its maximum symbol rate, through a filter with minimum tolerance bandwidth, according to $B_n = 9\,R_{sy}$ (noise bandwidth equals nine times symbol rate).

Filter noise bandwidths were also chosen such that a minimum number of filter bandwidths would cover the symbol rate range. The data estimate time constants (τ_D) were chosen in 1/3-decade increments so that IF filter bandwidth switching coincides with τ_D intervals.

IV. Phase-Locked Loop Design and SDA Performance Analysis

A. Design Characteristics

The subcarrier tracking loop shall be functionally configured as in Fig. 2 with the following design characteristics:

$$H(s) = \frac{G(s)}{1 + G(s)} = \frac{1 + 2T_2 s + T_2^2 s^2}{1 + s\left(\frac{1}{G} + 2T_2\right) + s^2\left(\frac{2T_1}{G} + T_2^2\right) + s^3\left(\frac{T_1^2}{G}\right)}$$

where

$G(s)$ = open loop transfer function $= \dfrac{G}{s}\dfrac{(1 + T_2 s)^2}{(1 + T_1 s)^2}$ (Ref. 1)

K_d = phase detector constant (V/cycle)

K_v = voltage-controlled oscillator (VCO) constant (Hz/V)

K_m = loop frequency multiplication factor

K_a = loop dc gain not included in loop filter

$G = \alpha_{sl} K_d K_v K_m K_a$

α_{sl} = loop gain suppression factor resulting from the effect of the bandpass limiter upon the amplitude error signal

$$= \text{erf}\left(\sqrt{\frac{(\alpha')^2}{8\pi B_{if}}\frac{S}{N_o}}\right) \text{for}\ v = 1/4$$

(see Fig. 1 and Ref. 2)

where v is the fraction of the strong signal peak error voltage at which the limiter saturates (Ref. 2), and, for a 50% transition probability (Ref. 2),

α' = loop gain suppression factor resulting from the data estimate action upon the loop

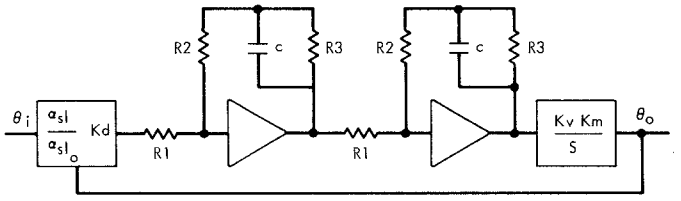
$$= \left[0.769\left(0.887 + 0.2\left(\frac{ST_{sy}}{N_o}\right)^{1.2}\right)\Big/ \left(1 + 0.2\left(\frac{ST_{sy}}{N_o}\right)^{1.2}\right)\right] \text{erf}\left(\left(0.667\frac{ST_{sy}}{N_o}\right)^{0.5}\right)$$

B. Loop Design Implementation

Since the doppler offset (Ω, Hz), doppler rate (Λ, Hz/s), and mission time (t, s) are known, the SDA static phase error can be solved for by:

$$\Phi_{ss} = \frac{360\,(\Omega + \Lambda t)}{G} + \frac{720\,\Lambda\,T_1}{G}\,(\text{deg})$$

Given the configuration shown below, the loop can be designed to meet the required steady state phase error (Φ_{ss}) for a particular application.



Since the loop filter has a transfer function of

$$F(s) = \left(\sqrt{K_a}\,\frac{1 + T_2 s}{1 + T_1 s}\right)^2 = \left(\left(\frac{R_2 + R_3}{R_1}\right)\left(\frac{1 + T_2 s}{1 + T_1 s}\right)\right)^2$$

then

$$T_1 = R3C = \frac{360T_2^3\,\Lambda}{q\,\phi_{ss}} + \sqrt{\left(\frac{360T_2^3\,\Lambda}{q\,\phi_{ss}}\right)^2 + \left(\frac{360T_2^3\,(\Omega + \Lambda t)}{q\,\phi_{ss}}\right)}$$

$$T_2 = R2C = \frac{q_o\,(2q_o + 3)}{2W1_o\,(2q_o - 1)}$$

where

$$q = \alpha_{sl}\left(\frac{K_d\,K_v\,K_m\,K_a\,T_2^3}{T_1^2}\right) \approx \alpha_{sl}\,K_d\,K_v\,K_m \times \left(\frac{R_2 + R_3}{R_3}\right)^2\left(\frac{R_2}{R_1}\right)^2 T_2$$

and

$$R_1 = R_2\left(\frac{R_2 + R_3}{R_3}\right)\sqrt{\frac{\alpha_{sl_o}\,K_d\,K_v\,K_m\,T_2}{q_o}}$$

C. Loop Design Characterization

1. Loop noise bandwidth (two sided) (Ref. 3)

$$\mathcal{W}_l = \frac{q\,(2q + 3)}{2T_2\,(2q - 1)} = \frac{r\,(4r + 3)}{T_2\,(4r - 1)}$$

where

$$r_o = \frac{GT_2^3}{2T_1^2} = \frac{q}{2} = 3.375\,(\text{Ref. 3})$$

$$r = r_o\,\frac{\alpha_{sl}}{\alpha_{sl_o}}\,(\text{Ref. 3})$$

Frequency acquisition can be accomplished by increasing the dc gain by a factor of 10 (bandwidth increase by a factor of 7.8) until frequency lock is accomplished and then logarithmically decreasing the gain to its nominal value.

2. Operating phase jitter. Theoretical phase noise of the subcarrier estimate is given by (Ref. 4):

$$\sigma_{\theta n}^2 = \Gamma_{sl}\left(\frac{1}{\alpha'}\right)^2\left(\frac{\pi}{2}\right)^2\left(\frac{N_o}{ST_{sy}} \times \frac{1}{2R_{sy}}\right) \times \left(\mathcal{W}_{l_o}\left(0.22447 r_o\,\frac{\alpha_{sl}}{\alpha_{sl_o}}\left(\frac{4r_o\,\alpha_{sl} + 3\alpha_{sl_o}}{4r_o\,\alpha_{sl} - 1\alpha_{sl_o}}\right)\right)\right)$$

where $r_o = 3.375$, and Γ_{sl} is the so-called soft limiter performance factor and may be taken as a constant 1.16 over the region of significant phase jitter (Ref. 5).

3. Signal-to-noise ratio degradation. Theoretical degradation of signal-to-noise ratio may be predicted as follows (Ref. 6):

$$\text{Degradation} = 20\log_{10}\left[1 - \left(\frac{2}{\pi}\right)^{1.5}\sigma_{\theta n} - \left(\frac{2}{\pi}\right) \times \phi_{ss}\,\text{erf}\left(\frac{\phi_{ss}}{\sqrt{2} \times \sigma_{\theta n}}\right)\right], \text{in dB}$$

where $\sigma_{\theta n}$ is as specified above and erf is the error function. Table 3 illustrates the four bandwidths that are available. The loop, in the "nonacquisition" mode, is critically damped, and is overdamped in the acquisition mode.

4. SDA performance. A software program (written in PDP-11 BASIC) is available that allows the user to define a particular mission (ST_{sy}/N_o, Ω_o, Λ_o, mission time, R_{sy} and f_{sc}) and the particular loop configuration ($\mathcal{W}_{l_o}$) to obtain total SDA degradation. To demonstrate what performance could be expected, two subcarrier frequencies (20 and 400 kHz) were chosen and total SDA degradation as a function of doppler rate was computed as the symbol rate was changed from 5 to 500 ksps. (Figs. 3, 4, 5).

V. Block IV SDA Loop Filter Dc Offset Analysis

Dc offset is always of concern in a phase-locked loop (either second or third order) since it is an important parameter in the acquisition and static phase error characteristics. The improved doppler rate tracking performance obtained in the Block IV SDA has been purchased by designing a third-order phase-locked loop. The third-order loop has reduced the long term stability requirements for the VCOs (due to higher loop gain and an improved acquisition characteristic) but has initiated the requirement for much better engineering of the dc stability problem.

Analysis was performed by Tausworthe to determine the effect on the dc offset problem.[1] Figures 6 and 7 are

[1]Tausworthe, R. C., Jet Propulsion Laboratory, Pasadena, Calif. (private communication).

plots of dc imperfection (E in mV, referred to the phase detector output) vs frequency offset for various bandwidths and represents the maximum frequency offset (for a particular dc imperfection) that the loop will drive toward a zero beat condition for the proposed Block IV SDA design.

Measurements were made on the prototype loop filter. The test data indicated a stability of 10 μV (referred to the phase detector output) is possible.

If a margin is assumed to cover manufacturing and adjustment, a 1-mV offset would guarantee the following performance at design point: The narrow band loop ($\mathcal{W}_{L_0} = 0.03$ Hz) will acquire from an offset of $4.6 \times \mathcal{W}_{L_0}$ and narrow bandwidth using auto acquisition will acquire from an offset of $30 \times (\mathcal{W}_{L_0} = 0.03\,\text{Hz})$. The wide bandwidth ($\mathcal{W}_{L_0} = 0.5$ Hz) will acquire from an offset of $16 \times \mathcal{W}_{L_0}$ and wide bandwidth using auto acquisition will acquire from an offset of $112 \times (\mathcal{W}_{L_0} = 0.5\,\text{Hz})$.

VI. Calibration Sequence and Configuration Control

A. General

The Block IV SDA can be controlled by an operator through the manual control panel or by a computer through the 14-line standard interface. The control unit (Fig. 8) allows three functions to be performed:

1. Automatic system calibration. Built-in digital hardware has the calibration logic programmed into it so that the SDA sequences through the necessary adjustments and tests to verify its operational status.

2. Configuration control. This allows Manual (or computer) control of all calibration and operational configurations.

3. Fault location. There are four features of the Block IV SDA that permit rapid fault location:

(1) Module status indicators (one for each module) indicate that all configuration relay and reference circuits are operating correctly. These indicators are normally off, and turn on when a failure occurs.

(2) A 3-bit alpha-numeric error indicator on the front panel indicates the step in the calibration sequence when a failure occurs.

(3) A voltmeter has been incorporated to monitor key test points.

(4) To test the indicators on the front panel, a special test function was designed into the unit. The "in-lock" indicator can be depressed, which causes all light emitting diode indicators to turn on, thus giving a test to the fault location indicators.

The three controls at the top left corner of the front panel are calibration sequence controls, (INT CAL, RCV1 CAL, and RCV2 CAL) which the operator can use to initiate automatic system calibration. If a receiver is in a strong signal (continuous wave) test condition, the SDA will adjust its phase and gain to match the particular receiver.

The configuration controls that are available are MOD INDEX (modulation index), SUBCARRIER FREQUENCY (X4), SYM RATE (symbol rate), and METER SELECT.

The MODE control switch selects between MAN (manual) and COMP (computer) control of the SDA. The NORMAL/INTERPLEX switch controls interplex phasing and insertion of a notch filter when appropriate. The INPUT selector allows either RCV1 (receiver 1) or RCV2 (receiver 2) or TAPE/TEST to be used as the input to the SDA. The OUTPUT selection for the SDA is either DEMOD, which is the SDA output, or TAPE or TEST, which are signals bypassing all but the output circuitry of the SDA. The LOOP controls select the loop bandwidth, initiate AUTO ACQ (auto acquisition) and place the loop in SHORT or in TRACK configuration.

The METER control allows a meter check by putting the ground on it. Measurements can be made to monitor the data or quad channel output, dynamic phase error, correlation detector output (also available on an analog meter), static phase error output or receiver 1 or 2 AGC voltage. The control unit thus serves as input into, and receives feedback from, the SDA so that the indicators on the front panel reflect the static and dynamic status of the system.

B. SDA Control Unit Logic Description

The logic flow of the Block IV SDA is described in the following pages and is shown as a logic flow diagram in Fig. 9.

1. Momentary power loss. The SDA control unit contains a "power on" sensing circuit that is utilized to indicate a momentary loss of power. This feature is important because information stored in the SDA control registers

can be lost as a result of a power loss. The operation of the "power on" sensing electronics is as follows:

(1) When the power drops below an adequate level, the computer data-ready line is pulled down (grounded). This condition would be apparent on the control panel as erratic indications from indicator/switches.

(2) When the power comes back up to an acceptable level, the "power on" sensing circuit sends a signal to the computer and control panel ERROR WORD display, indicating there has been a power loss. This indicates to the computer or operator that there has been a power loss and the full calibration procedure must be initiated.

(3) The "power on" signal also initiates the following:

(a) Power on time delay (1 min).

(b) Internal voltage test. The control unit configures itself to measure internal voltages. The successful completion of this function provides an enable for the INT CAL command.

(c) Set configuration word flag to NO. This prevents the SDA from using the stored computer configuration word if there had been a momentary power loss. When the computer sends the configuration word the flag is changed to YES.

2. Calibration summary. The calibration of the SDA is composed of two major functions: internal calibration and receivers 1 and 2 calibration. Internal calibration is performed using no external input signals (except 5- and 10-MHz reference) and receivers 1 and 2 calibration utilizes a 10-MHz (continuous wave) signal from the receivers. The SDA control unit automatically performs the calibration procedure, adjusting SDA module parameters so the SDA is ready to receive the spacecraft signal. The sequencing of the SDA into and out of these major calibration functions is presented on the following pages. The tuning operations performed during calibrations are listed below.

a. Internal calibration

(1) Phase adjust: adjusts phase shifters for output null for the data channel, quad channel, and error channel.

(2) Gain adjust: adjusts attenuators for nominal output for the data channel and quad channel.

(3) Phase check: verifies output null for all gain/bandwidth settings for the data channel, quad channel, and error channel.

(4) Gain check: verifies nominal output for all gain/bandwidth settings for the data channel, quad channel, and error channel.

(5) Interplex test: verifies interplex 90-deg phase shifter is functioning.

(6) Loop check: generates subcarrier (f_{sc}) times data test signal to check loop acquisition performance.

(a) Normal acquisition: checks acquisition for the 0.5-Hz and 0.23-Hz bandwidths.

(b) Auto acquisition: checks auto acquisition in wide (3.9-Hz to 0.5-Hz) bandwidths.

b. Receivers 1 and 2 calibration

(1) Adjust phase: adjusts SDA phase for operation with receivers 1 and 2.

(2) Adjust gain: adjusts SDA gain for operation with receivers 1 and 2.

VII. Mechanical Design and Thermal Analysis

The required subassemblies, for two Block IV SDAs, are mounted in a standard DSN 209-cm (82.31-in.) high rack cabinet. The various units have been distributed with the largest heat dissipation assemblies located at the top. The two synthesizers and SDA modules have been located toward the bottom of the cabinet to optimize their local temperature environment to guarantee performance. The two Control Units and associated Manual Control Panels are located at eye height, for operator convenience (see Fig. 10).

The front door of the cabinet will be normally closed to prevent cooling air loss. A bezel and cutout in the front door provide operator access to the two manual control panels, without opening the door, and provide the necessary cooling air seal.

Cooling air will be provided by two standard DSN rack cabinet side ducts. These will be modified by removing 7.6 cm (3 in.) from the bottom of the inside face and angling an air scoop, at approximately 45 deg, from the rack bottom, into each side duct. It is anticipated that this modification will reduce air flow resistance into the side ducts. All other air flow into the cabinet will be blocked by the connector interface plate mounted in the cabinet bottom.

Dc power requirements have been measured or approximated based on breadboard measurements, and the power supply efficiency has been measured vs load. From

these, the total SDA power dissipation was estimated. Thermal analysis indicates that with cabinet heat dissipation of approximately 1230 W and 15°C station plenum inlet air temperature, the temperature at the cabinet top outlet will be approximately 25°C.

VIII. Status of Design and Engineering Model Development

A. Design Status

Seven out of the ten module types have been documented to the point of having printed circuit (PC) board masters and machine drawings. Photographic techniques are planned to make all subassembly and assembly drawings to reduce documentation costs. The three remaining modules are scheduled for completion of design by June 1973.

B. Engineering Model

All module types have been prototyped and present plans call for an engineering model (containing PC boards made from released documentation) in August 1973. This engineering model will be used to confirm the design and serve as an example at the bidders' conference to better describe the procurement package.

It is planned to be on contract by October 1973 and deliver two SDAs to DSS 14 in August 1974, and the remaining two SDAs to DSS 43 in November 1974.

References

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3. Brown, D. H., "Third-Order Phase-Locked Loop Perspectives," in *The Deep Space Network Progress Report*, TR 32-1526, Vol. VIII, pp. 99–110. Jet Propulsion Laboratory, Pasadena, Calif., April 15, 1972.
4. Brockmann, M. H., "MMTS: Performance of Subcarrier Demodulator," in *The Deep Space Network*, Space Programs Summary 37-52, Vol. II, p. 134, Eq. (34). Jet Propulsion Laboratory, Pasadena, Calif., July 31, 1968.
5. Tausworthe, R. C., "Analysis of Narrow-Band Signals Through the Band-Pass Soft Limiter," in Supporting Research and Advanced Development, Space Programs Summary 37-53, Vol. III, pp. 209–214. Jet Propulsion Laboratory, Pasadena, Calif., Oct. 31, 1968.
6. Brockmann, M. H., "MMTS: Performance of Subcarrier Demodulator," in *The Deep Space Network*, Space Programs Summary 37-52, Vol. II, p. 134, Eq. (35). Jet Propulsion Laboratory, Pasadena, Calif., July 31, 1968.
7. Crow, R. B., Holmes, J. K., and Tausworthe, R. C., "Block IV Subcarrier Demodulator Assembly Acquisition Problem," in *The Deep Space Network Progress Report*, TR 32-1526, Vol. XIII, p. 42. Jet Propulsion Laboratory, Pasadena, Calif., Feb. 15, 1973.

Table 1. Functional comparison between Block III and Block IV SDA

Function	Block III	Block IV	Comments
Symbol rate	5.6 to 270 k symbols per second (sps)	5.6 to 500 ksps	Required for Mariner Jupiter/Saturn 1977 (MJS'77)
Subcarrier frequency	100 Hz to 1 MHz	100 Hz to 1 MHz	
Tracking loop type	2nd order	3rd order	Improves SDA performance in the presence of high loop stress due to doppler rate (i.e., Jupiter flyby)
Modulation index range	10 to 74 deg (2-dB resolution)	10 to 80 deg (1-dB resolution)	User requested mod index range increase
τ_0	5.6 to 5.6 ksps	5.6 to 120 sps	This output limited to 56 sps by the Telemetry and Command Processor Assembly (TCP)
SDA input bandwidth (−1 dB)	3 MHz	7 MHz	To be compatible with Block IV receiver
Interplex operation	Manual phasing, no monitor, no notch filter	Phasing, monitoring, notch filter controlled by firmware	To reduce operator involvement and improve performance
Controls	Manual	Manual/computer	To reduce operator involvement and improve performance
Monitor	Manual/computer	Manual/computer	
Alignment	Manual	Firmware	To reduce operator involvement and improve performance
Size	Full standard equipment rack	Half of standard equipment rack	Cost reduction
Auxiliary (acquisition)	Part of design	Not included	Not used on Block III
BER data feedthrough	Part of design	Not included	
1 MHz output	Part of design	Not included	
Reference frequency			
Input	5, 10 MHz	5, 10 MHz	
Output from synthesizer	5 MHz	5 and 10 MHz	
Internal frequency standard in synthesizer	Yes	(5-MHz stations reference to be used)	Cost reduction
Incidental SDA degradation	0.1 ±0.1 dB	0.1 ±0.1 dB	
DC offset and stability	0 ±5 mV (per day)	0 ±5 mV	Reduce calibration requirement

Table 2. Design differences between Block III and Block IV SDA

Function	Block III	Block IV	Comments
Loop bandwidth	0.03, 0.15, 0.375, 1.5 Hz	0.03, 0.234, 0.5, 3.9 Hz	
Acquisition scheme	0.15 to 0.03 Hz, automatic when loop locks, no acquisition for 0.375- or 1.5-Hz loop	0.234 to 0.03 Hz, or 3.9 to 0.5 Hz logarithm bandwidth reduction when loop lock; can operate in acquisition bandwidth as an operational configuration (Ref. 7)	
Soft limiter suppression factor ν	1/2	1/4	This increases the radio-frequency (RF) loop gain (therefore minimizes the dc loop gain) to optimize the total dc stability
Bandwidth of soft limiter	500 Hz	1.0 kHz	500-Hz bandwidth at 10 MHz has proven too costly in Block III SDA
Signal to subcarrier leakage ratio	16 dB at 110 kHz 9 dB at 1.1 MHz	27 dB at 110 kHz 19 dB at 1.1 MHz	Reduce unwanted (additive) subcarrier signal
Internal SDA signal-to-noise ratio			
Data channel	+17 dB	+21 dB	Better internal noise characteristics permit easier calibration and trouble diagnostics
Error channel	+40 dB	+58 dB	
IF system linearity			
Design point $\frac{ST_{sy}}{N_o}$	−1 dB ($5.6 < R_{sy} < 270$ ksps)	−1 dB ($5.6 < R_{sy} < 480$ sps) −4 dB ($480 < R_{sy} < 500$ ksps)	
Receiver 1/2 AGC voltage	Not required	Required by firmware control	
In-lock detector sensitivity $\left(\frac{ST_{sy}}{N_o}\right)$	−1 dB	−1 dB	

Table 3. Subcarrier tracking loop parameters

Loop bandwidth	$\mathcal{W}_{l_o}^{1,2}$, Hz	$G_o^{1,3}$, $\mathcal{W}$ 1/s	K_{DO}^5, V/90 deg	K_{VCO}, Hz/V	T_1, s	T_2, s
Narrow	0.03	56.8	0.034	1	5250	148.5
Narrow acquisition[5]	0.234	568	0.034	1	5250	148.5
Wide	0.5	263,020	0.143	10	5250	8.91
Wide acquisition	3.90	2,630,200	0.143	10	5250	8.91

[1]Design point chosen for uncoded limiter suppression factor, $\alpha_o' = 0.48$

[2]IF limiter-detector characteristics for $S/N_o = +8$ dB, +19 dB

[3]K_M (quadrature generator) = 0.25

[4]$\nu = \frac{1}{4}$; $K_{D_{strong\ signal}} = 4$ V/90 deg

[5]Acquisition mode can be used as a tracking bandwidth, or can be commanded to logarithmically reduce the bandwidth to its nominal value (i.e., narrow or wide). The acquisition amplifier has a nominal gain of 20, which is increased to 200 in the acquisition mode.

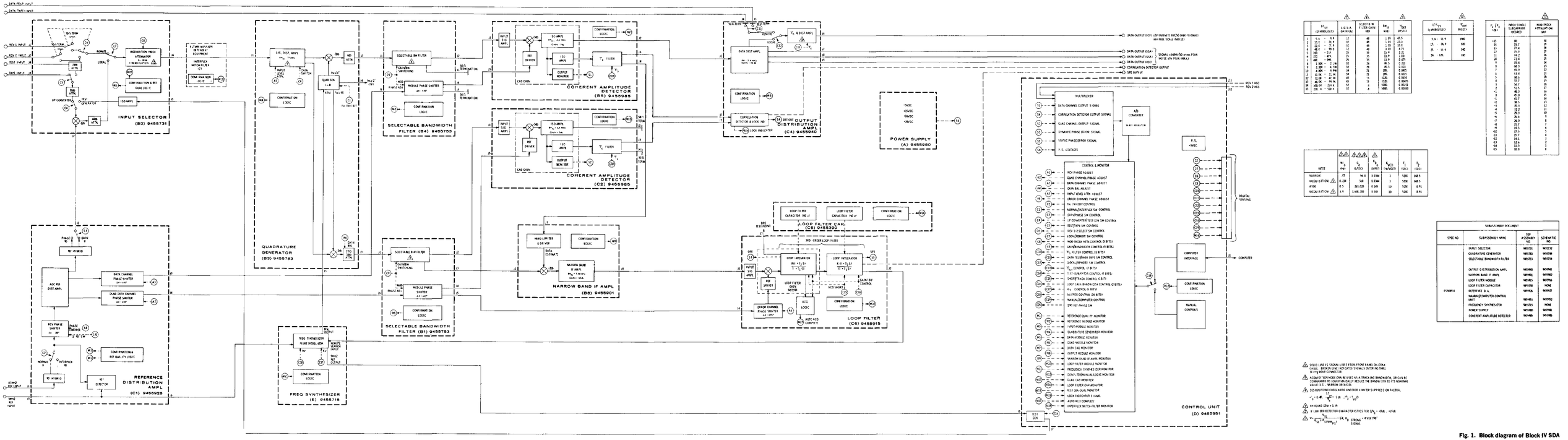

Fig. 1. Block diagram of Block IV SDA

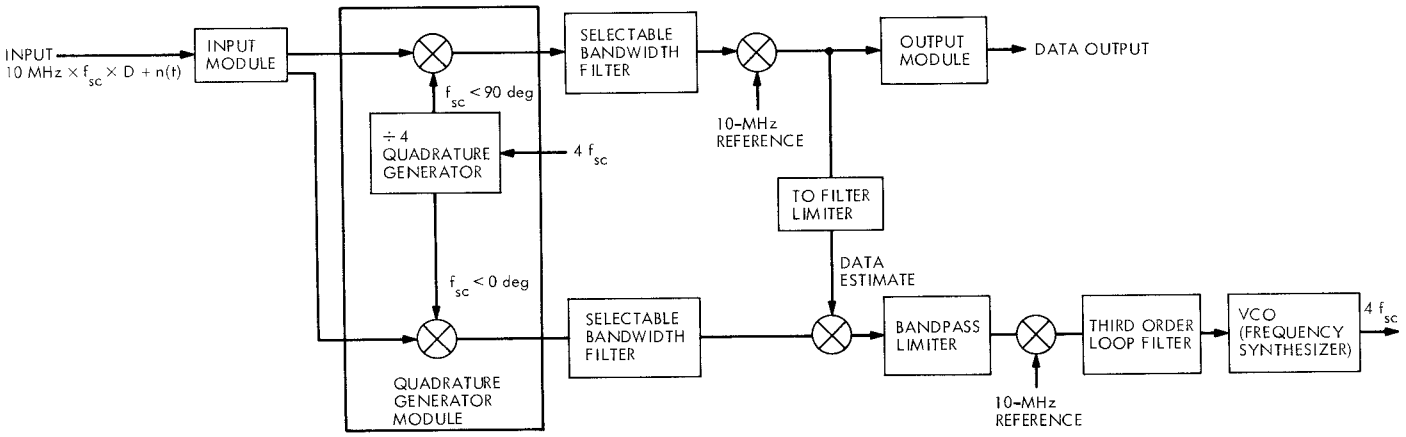

Fig. 2. Subcarrier tracking loop

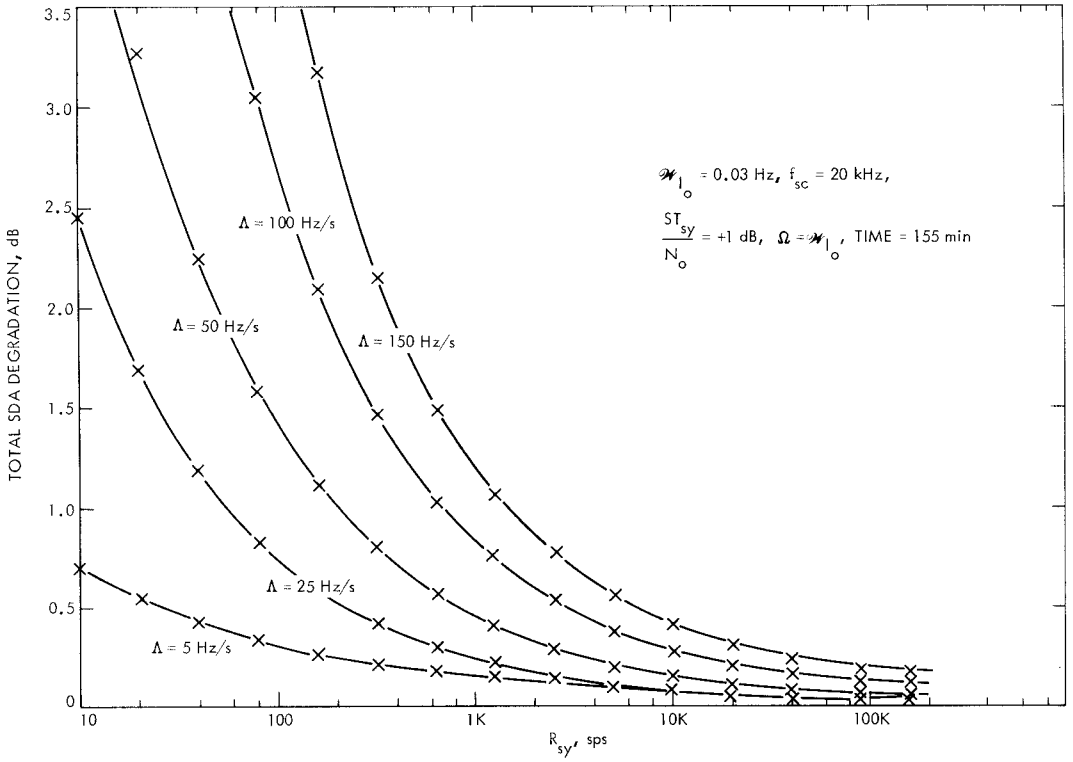

Fig. 3. Total SDA degradation vs R_{sy}; $\mathcal{W}_{I_o} = 0.03$ Hz, $f_{sc} = 20$ kHz

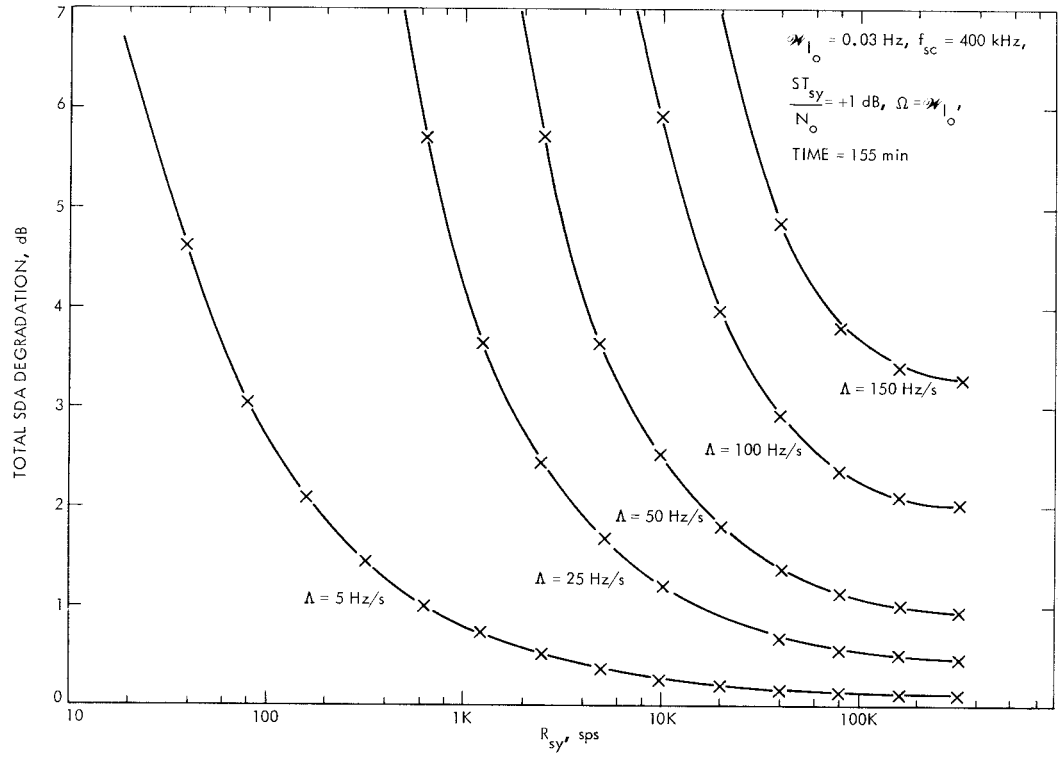

Fig. 4. Total SDA degradation vs R_{sy}; $\mathcal{W}_{I_o}$ = 0.03 Hz, f_{sc} = 400 kHz

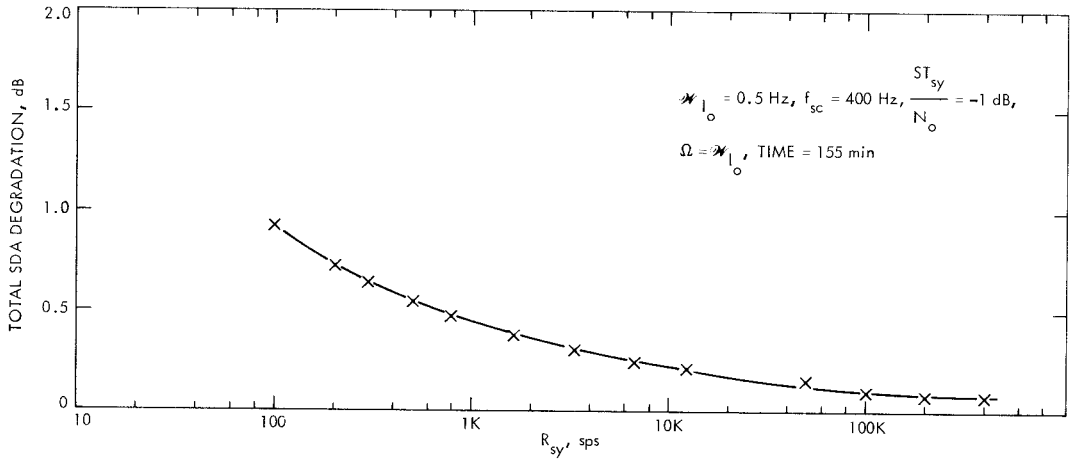

Fig. 5. Total SDA degradation vs R_{sy}; $\mathcal{W}_{I_o}$ = 0.5 Hz, f_{sc} = 400 kHz

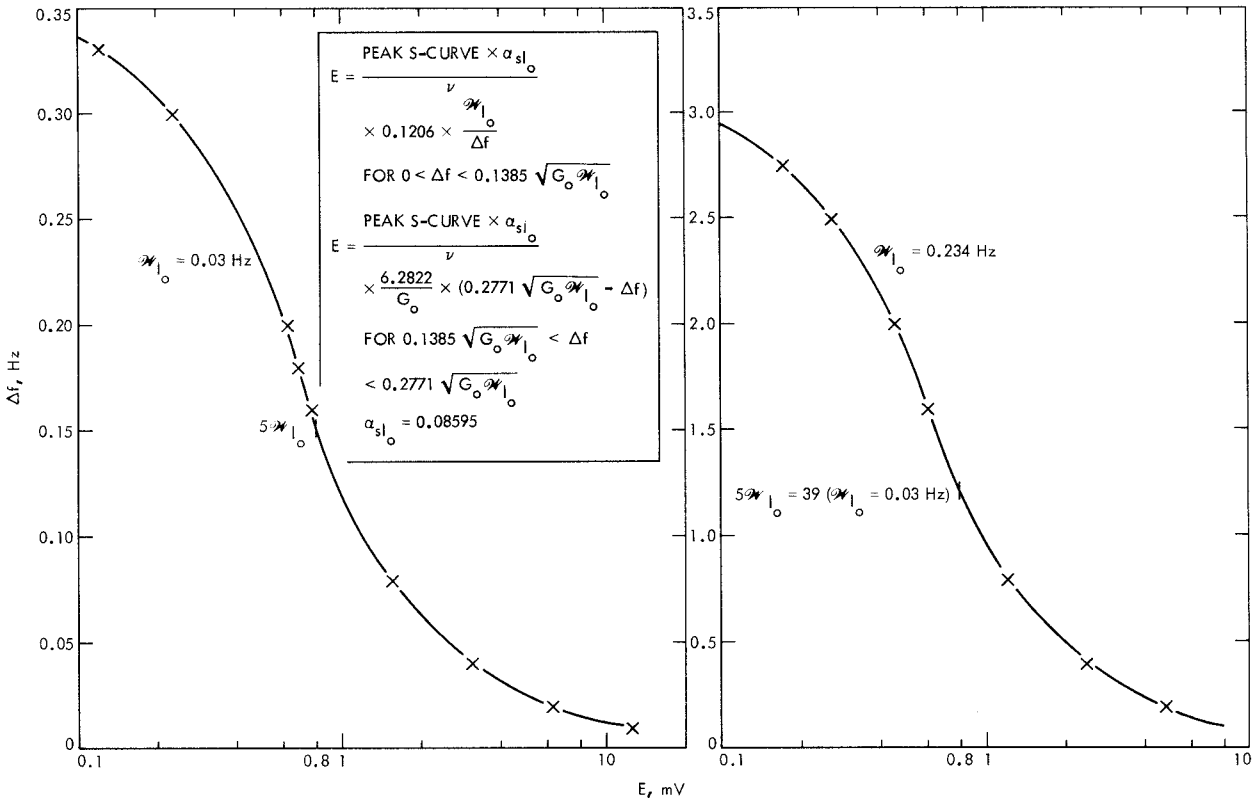

Fig. 6. Acquisition Range vs dc imperfection; $\mathscr{W}_{l_o}$ = 0.03 Hz

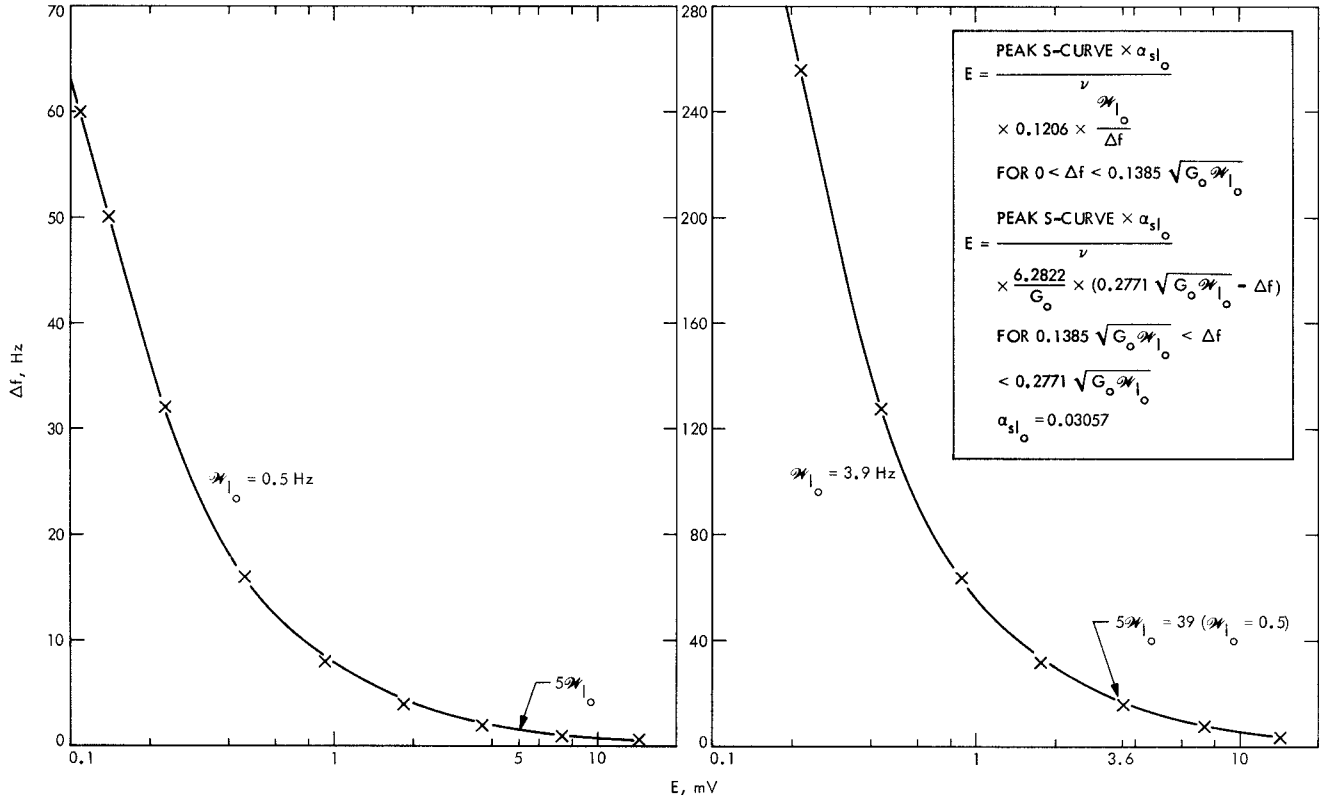

Fig. 7. Acquisition Range vs dc imperfection; $\mathscr{W}_{l_o}$ = 0.5 Hz

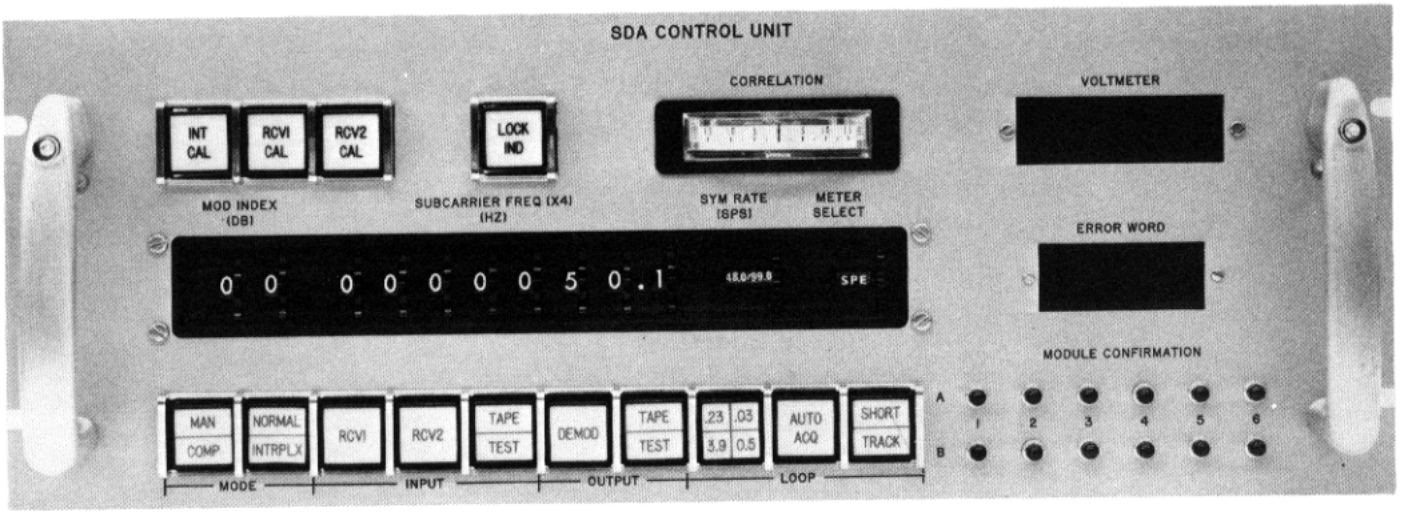

Fig. 8. Block IV SDA control panel

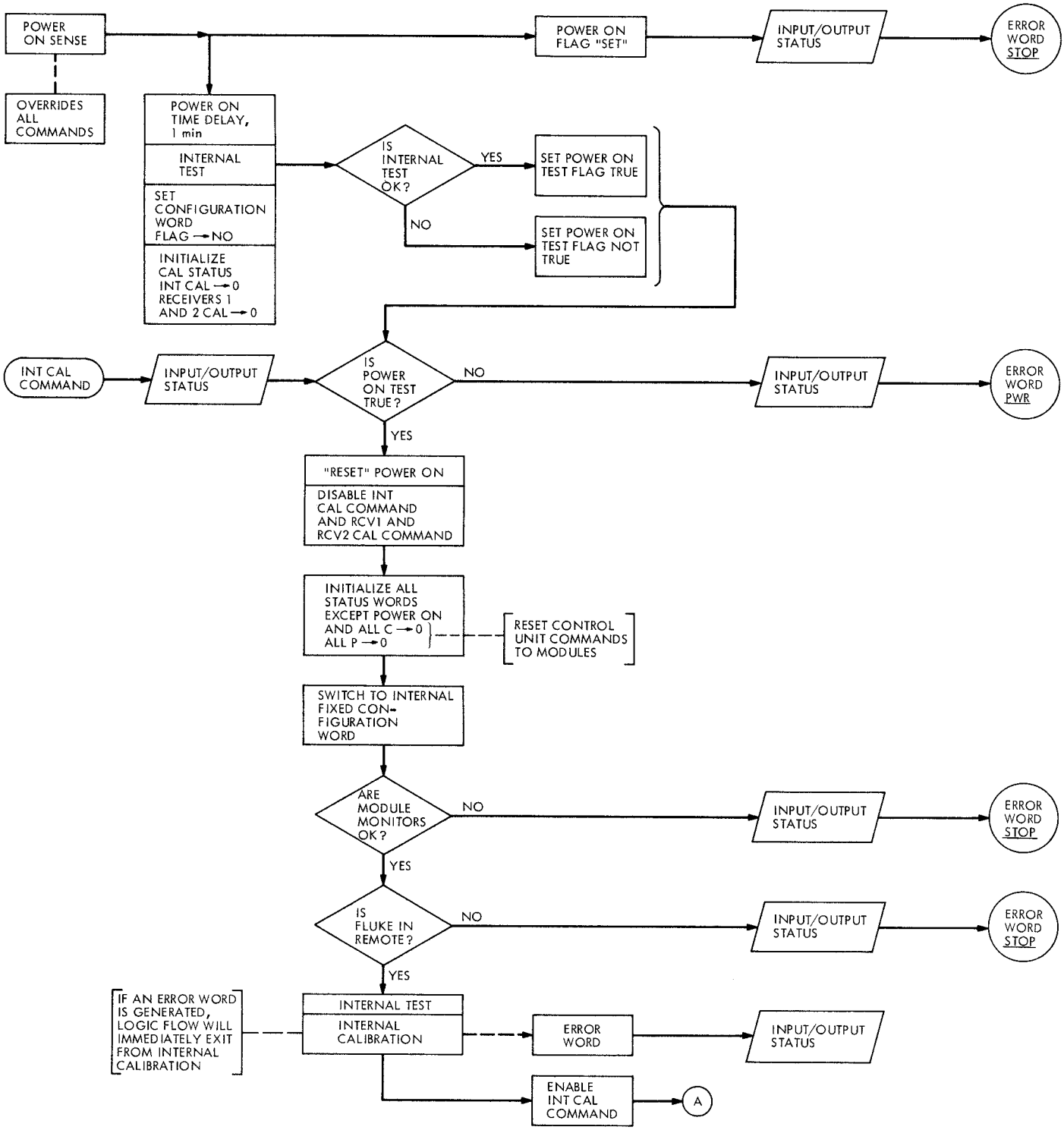

Fig. 9. Block IV SDA control unit logic flow diagram

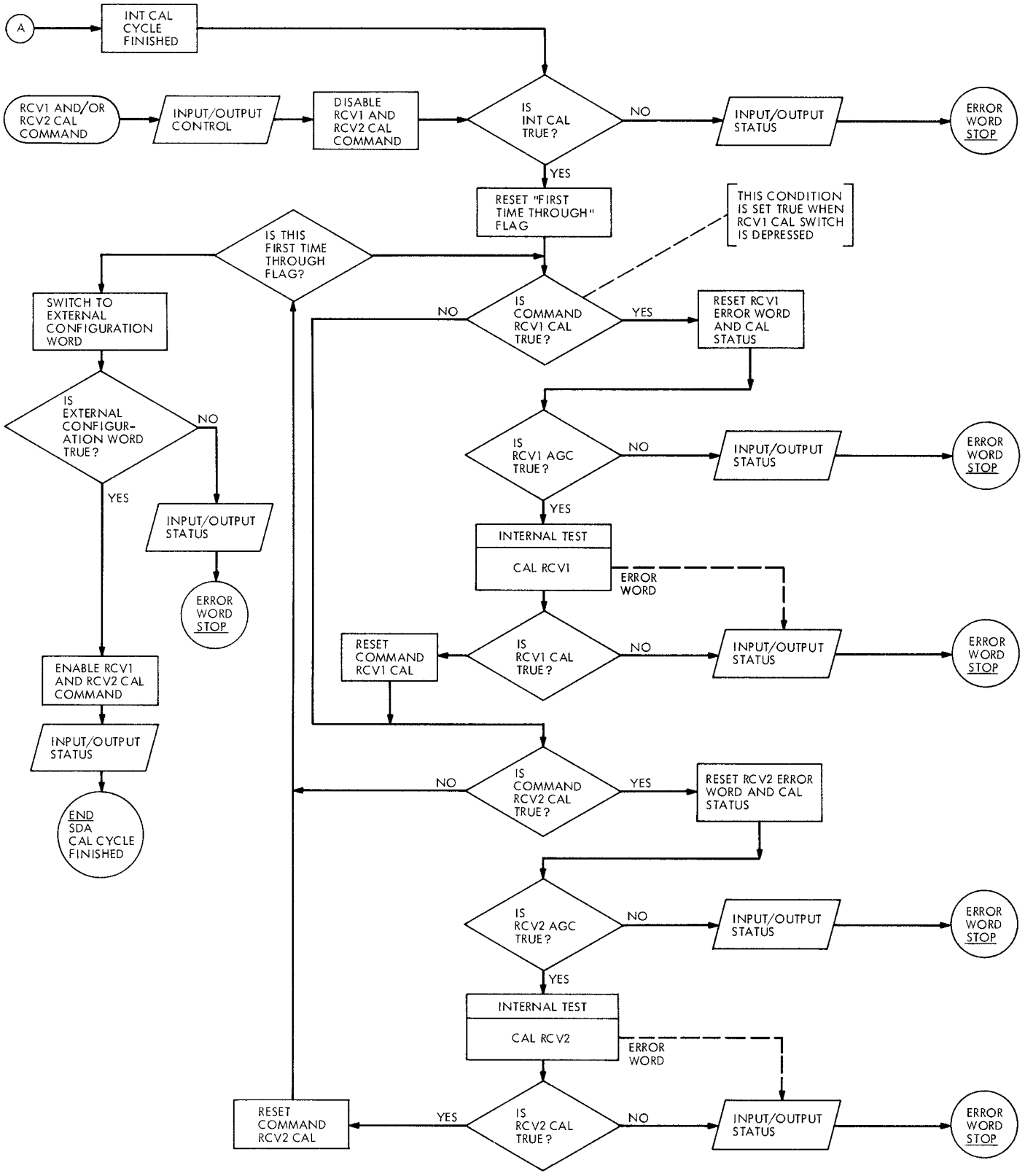
A
INT CAL CYCLE FINISHED
RCV1 AND/OR RCV2 CAL COMMAND
INPUT/OUTPUT CONTROL
DISABLE RCV1 AND RCV2 CAL COMMAND
IS INT CAL TRUE?
NO
INPUT/OUTPUT STATUS
ERROR WORD STOP
YES
RESET "FIRST TIME THROUGH" FLAG
THIS CONDITION IS SET TRUE WHEN RCV1 CAL SWITCH IS DEPRESSED
IS THIS FIRST TIME THROUGH FLAG?
SWITCH TO EXTERNAL CONFIGURATION WORD
IS COMMAND RCV1 CAL TRUE?
NO
YES
RESET RCV1 ERROR WORD AND CAL STATUS
IS EXTERNAL CONFIGUR-ATION WORD TRUE?
NO
YES
INPUT/OUTPUT STATUS
ERROR WORD STOP
IS RCV1 AGC TRUE?
NO
INPUT/OUTPUT STATUS
ERROR WORD STOP
YES
INTERNAL TEST
CAL RCV1
ERROR WORD
ENABLE RCV1 AND RCV2 CAL COMMAND
INPUT/OUTPUT STATUS
END SDA CAL CYCLE FINISHED
RESET COMMAND RCV1 CAL
IS RCV1 CAL TRUE?
NO
INPUT/OUTPUT STATUS
ERROR WORD STOP
IS COMMAND RCV2 CAL TRUE?
NO
YES
RESET RCV2 ERROR WORD AND CAL STATUS
IS RCV2 AGC TRUE?
NO
INPUT/OUTPUT STATUS
ERROR WORD STOP
YES
INTERNAL TEST
CAL RCV2
ERROR WORD
RESET COMMAND RCV2 CAL
YES
IS RCV2 CAL TRUE?
NO
INPUT/OUTPUT STATUS
ERROR WORD STOP

Fig. 9. (contd)

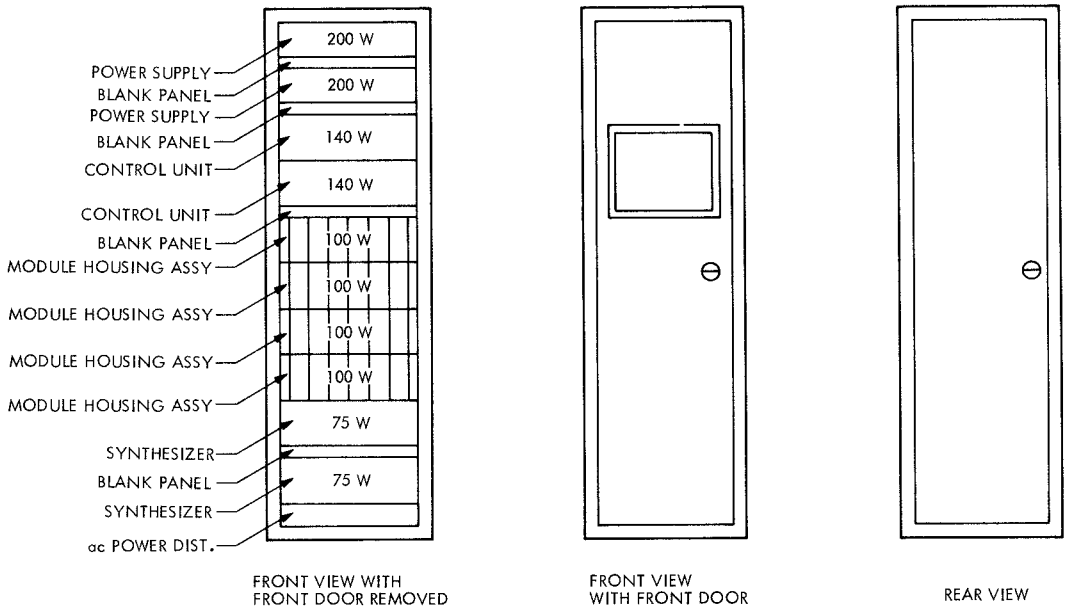

Fig. 10. SDA rack configuration