Digital DC Offset Compensation of Analog-to-Digital Converters

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A digital dc offset restoration system is described for use with wide bandwidth analog-to-digital converters (ADC). The main feature is that the system compensates for offsets in the conversion device itself, as well as for analog input offsets. A 1-bit ADC realization is described which operates at 40 Mbps using transistor-transistor logic in the dc restore circuitry. Conversion rates of over 100 Mbps can be achieved using emitter-coupled logic exclusively. This high-speed ADC is used in spectral analysis of planetary radar returns.

I. Introduction

A digital dc offset compensation system is presented for use with analog-to-digital (A/D) conversion systems. The system is described with application to a 1-bit A/D converter used in a planetary radar spectral analysis system. The application easily extends to higher-resolution converters in other data acquisition systems. The system has two major advantages over conventional analog techniques such as capacitor or transformer coupling: first, the frequency response of the system does not depend on the characteristics of a capacitor or transformer high-pass filter; and second, offsets in the converter itself are compensated for, as the final digitized signal, rather than just the analog input, is ensured to have zero offset.

The digital feedback used to compensate for input offsets utilizes an up/down counter (UDC) to integrate the converter output. The integrator output is fed back to the converter input through a digital-to-analog (D/A) converter and an amplifier. The system stabilizes when, on the average, the ADC output has an equal number of plus ones and minus ones. The UDC used in the feedback not only compensates for but measures the input offsets digitally, since the offset is linearly related to the digital value stored in the counter.

Application of the restoration technique to higher-resolution converters is accomplished by replacing the first stage of the UDC with an adder and accumulator, with overflow to the UDC.

II. Mathematical Model

Figure 1 shows a linearized model of the A/D converter with dc restoration. The effect of the limiter is assumed to be only a gain. To determine this gain, assume that the

input is zero mean gaussian noise with rms voltage σ, plus a small signal $s(t)$, with $s(t) << \sigma$. Then at any time the expected value of the limiter output is

$$\sqrt{\frac{2}{\pi}}\frac{1}{\sigma}s(t)$$

so the limiter gain is

$$K_L = \sqrt{\frac{2}{\pi}}\frac{1}{\sigma} \tag{1}$$

The up-down counter and D/A converter act as an integrator. The gain of an integrator is the voltage change in one second when the input is 1. If the counter has N total stages, and the D/A converter output voltage range is from $-V$ to $+V$ volts, then the output voltage changes $2^{-N}(2V)$ volts at each count. Since there are $1/T$ counts per second, the gain is

$$K = 2^{1-N}\left(\frac{V}{T}\right) \tag{2}$$

The closed-loop transfer function of the linearized system is

$$\frac{e_o(S)}{e_i(S)} = \frac{K_L}{1+\frac{K_L K}{S}} \tag{3}$$

This is equivalent to an RC high-pass filter with gain K_L and cutoff frequency $K_L K$ rad/s. In terms of the system parameters, the cutoff frequency is

$$f_c = \frac{1}{\pi}\sqrt{\frac{2}{\pi}}\frac{2^{-N}}{\sigma}\frac{V}{T}\text{ Hz} \tag{4}$$

It is important to note that the cutoff frequency is inversely proportional to the rms input voltage.

III. Implementation

Figure 2 is a block diagram of the converter which was constructed using the dc offset compensation. The high-speed comparator and clock shaper are Advanced Micro Devices AM68534E. Used as 1-bit A/D converters, these emitter-coupled logic (ECL) circuits have an aperture time of only 0.4 ns. The converter outputs were translated from ECL to transistor-transistor logic (TTL) levels, and the high speed U/D controller and UDC were constructed with TTL. This enabled the required clock rate of 40 MHz. Clock rates in excess of 100 MHz could be achieved using ECL exclusively.

The high-speed U/D controller operates on the serial input bits in pairs. It generates one up clock pulse to the UDC if both bits of a pair are plus one, a down clock pulse if both are minus one, and no clock pulse if the two bits are different. The effect is to act as an additional counter stage and to reduce the clock rate to the UDC integrated circuit (IC) chips by a factor of 2. The controller also keeps the 16-bit UDC from overflowing if the offset number is too great by inhibiting counting for minimum and maximum values of the counter.

The 12 most significant bits (MSB) of the UDC go to an Analog Devices "L" series Minidac. A Teledyne Philbrick 131901 is used as the level adjusting feedback amplifier. It was set for a gain of 2. Since the dc restore signal is applied to the negative input of the differential comparator, its voltage, when stabilized, is equal to the input offset voltage plus any offset introduced in the converter.

IV. Experimental Results

The 1-bit converter was operated at a 40-MHz clock rate over a wide range of input offsets and spectral components. Figure 3 is a photograph of the low-frequency portion of the output spectral density when the input signal was wideband gaussian noise, low-pass-filtered to 20 kHz to be within the bandwidth of the spectrum analyzer. The input signal level was 0.6 V rms, which, from Eq. (4), results in a calculated 3-dB cutoff frequency of $f_c = 250$ Hz. The measured spectral density agrees with this to within the resolution of the display.

V. Conclusion

The main feature of the dc restoration technique is its ability to correct for dc offsets introduced by the conversion device itself as well as for large dc offsets in the input signal. Using emitter-coupled logic for the filtering as well as for the converter, the dc restoration technique could operate at the highest conversion rates possible with the A/D converter chip, which is in excess of 100 MHz.

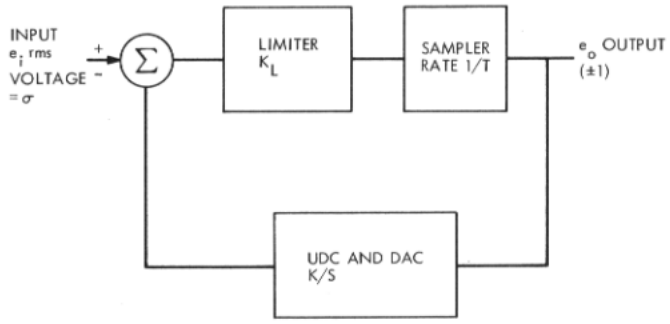

Fig. 1. Linearized model of ADC with digital dc restorer

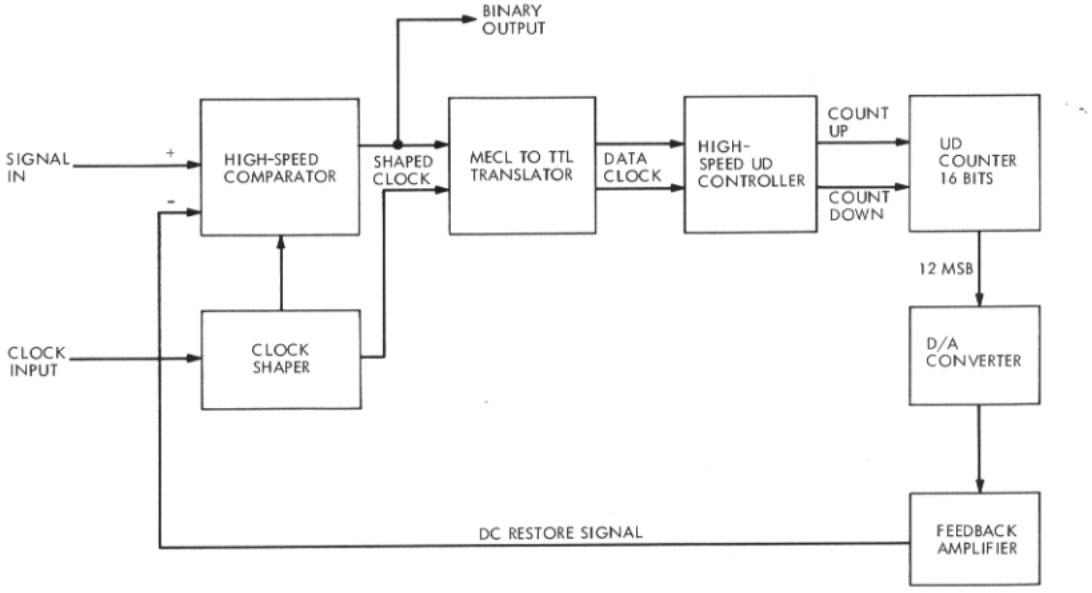

Fig. 2. Block diagram of the 1-bit ADC with digital dc restorer

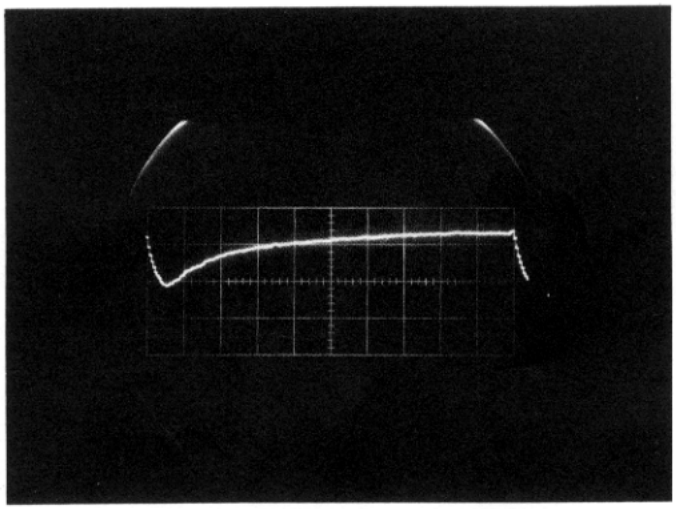

Fig. 3. A/DC low-frequency output spectral density (horizontal, 50 Hz/cm; vertical, 10 dB/cm)